

Fig. 1

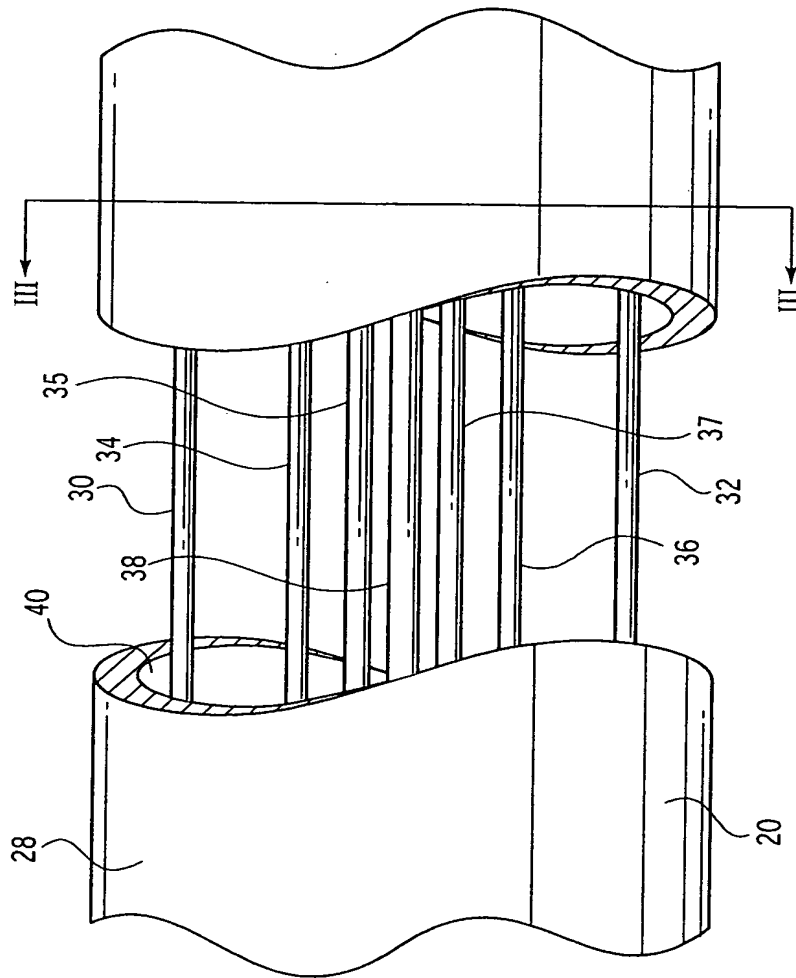


Fig. 2

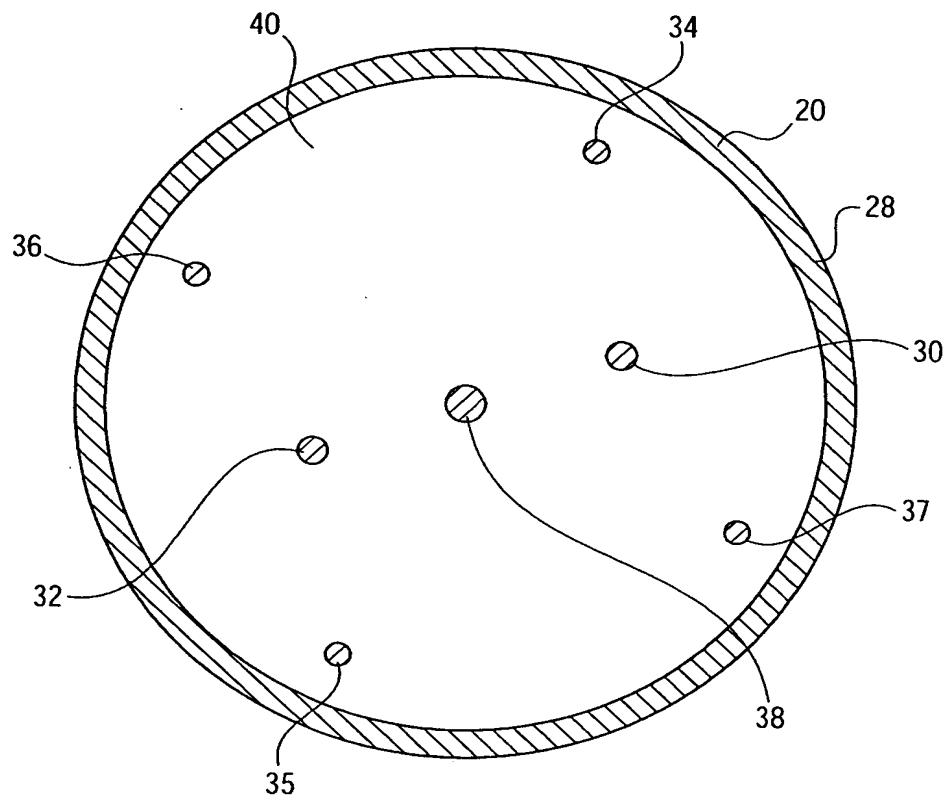


Fig. 3

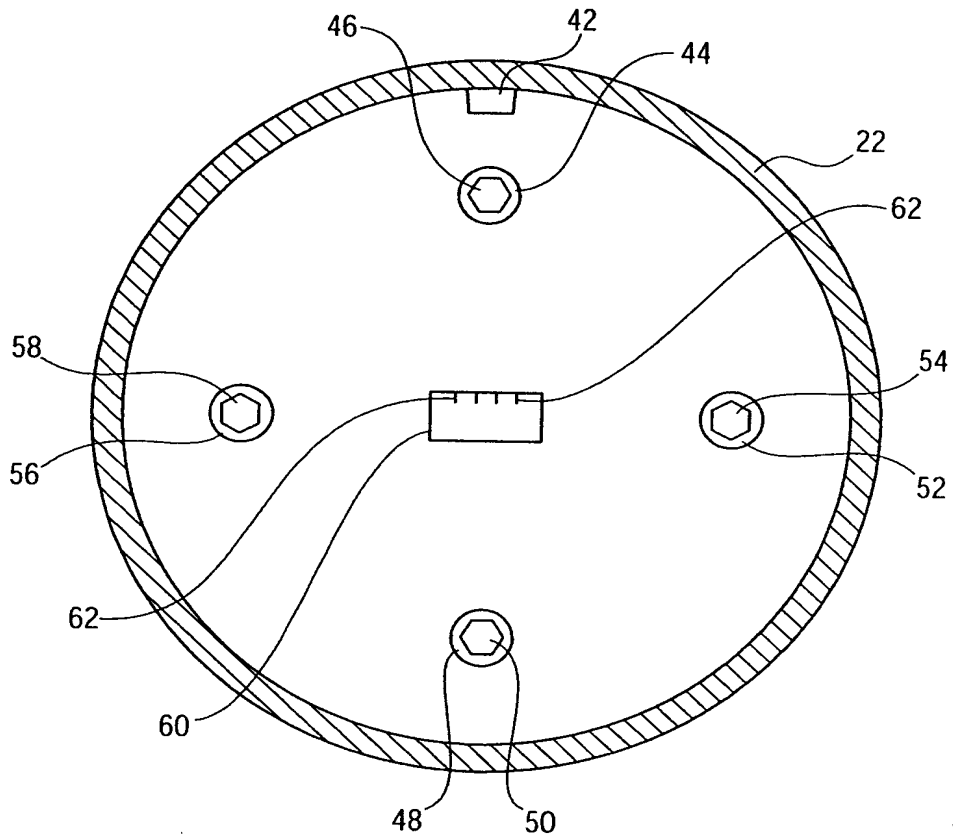


Fig. 4

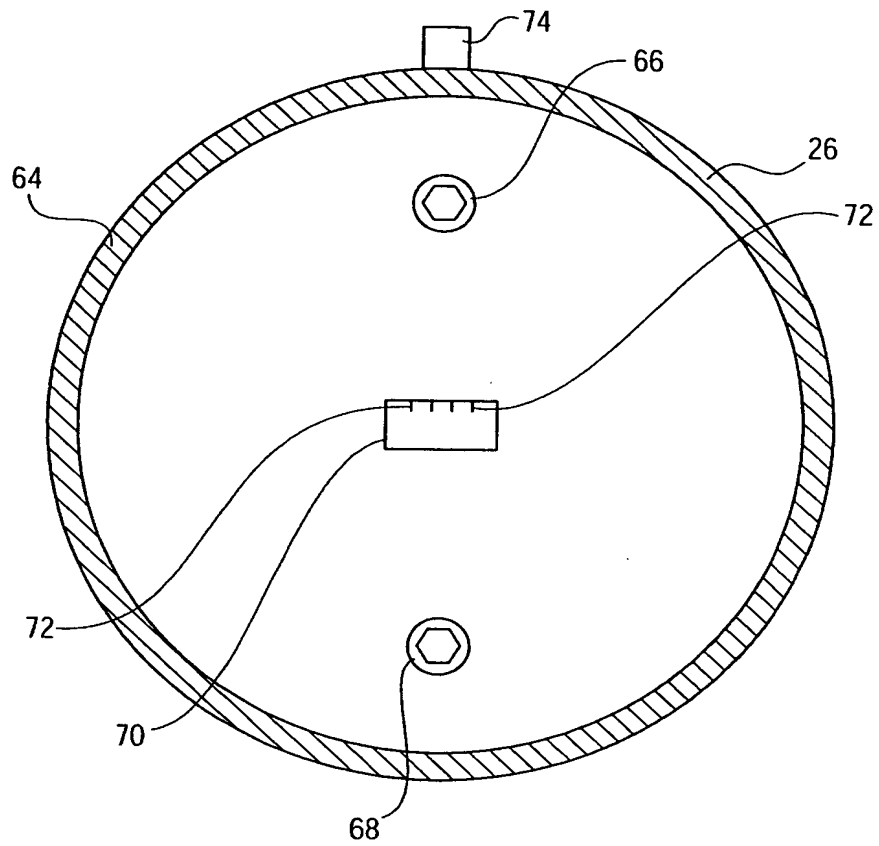


Fig. 5

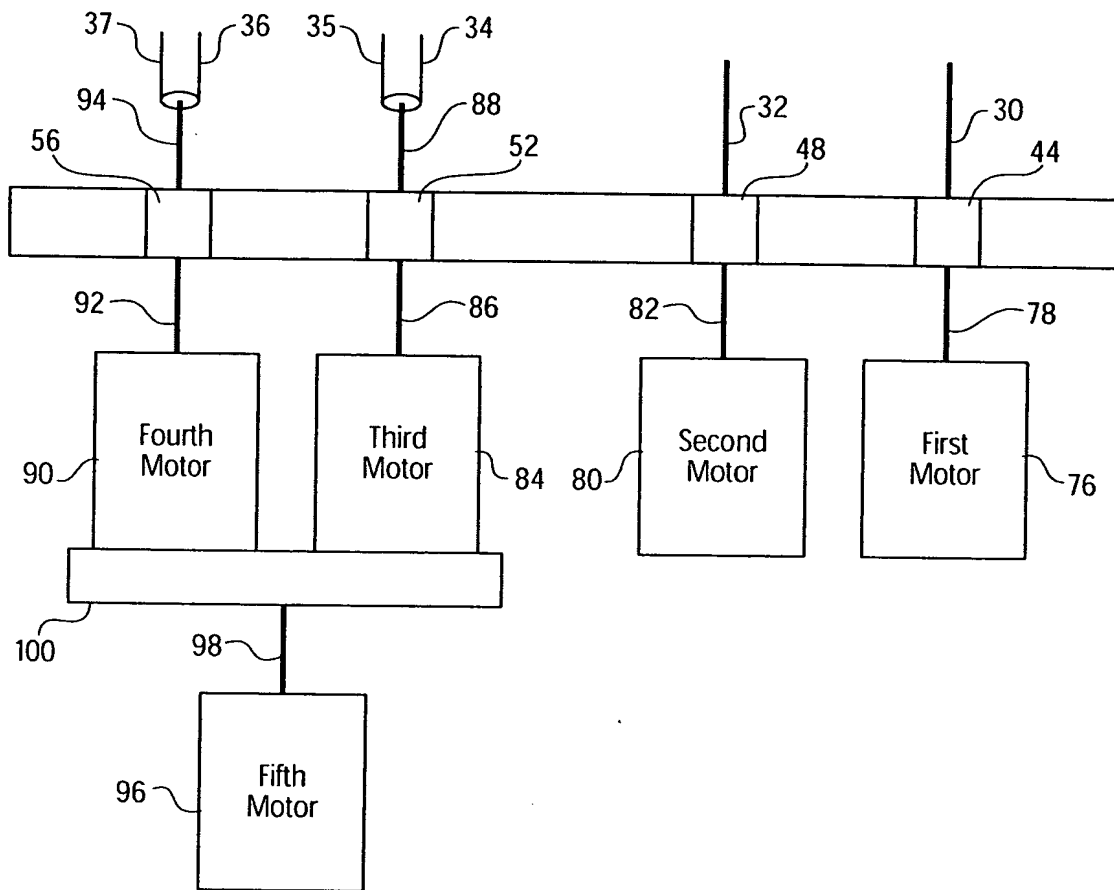


Fig.6

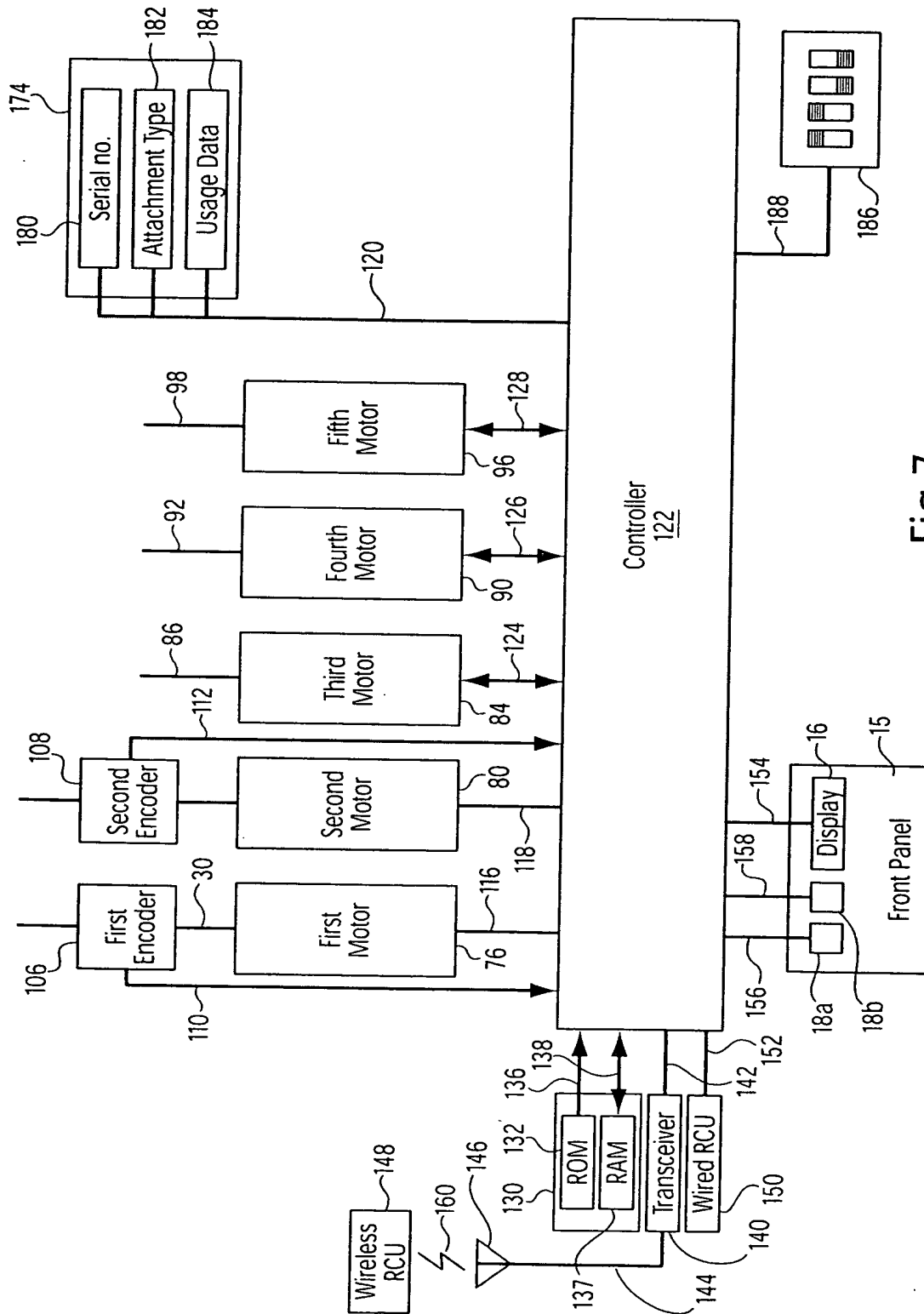


Fig. 7

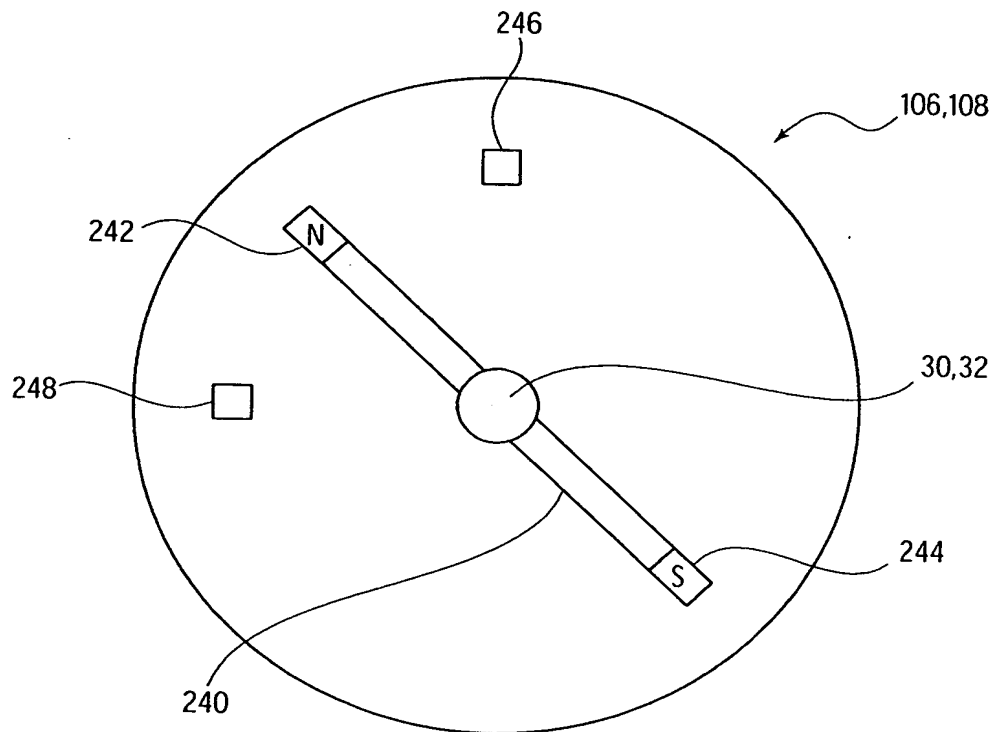


Fig. 8

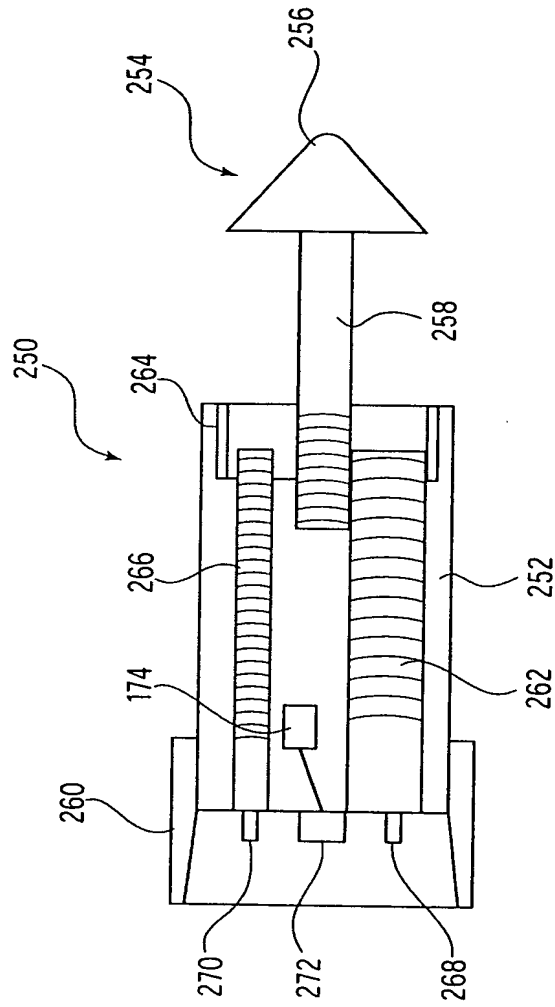


Fig. 9A

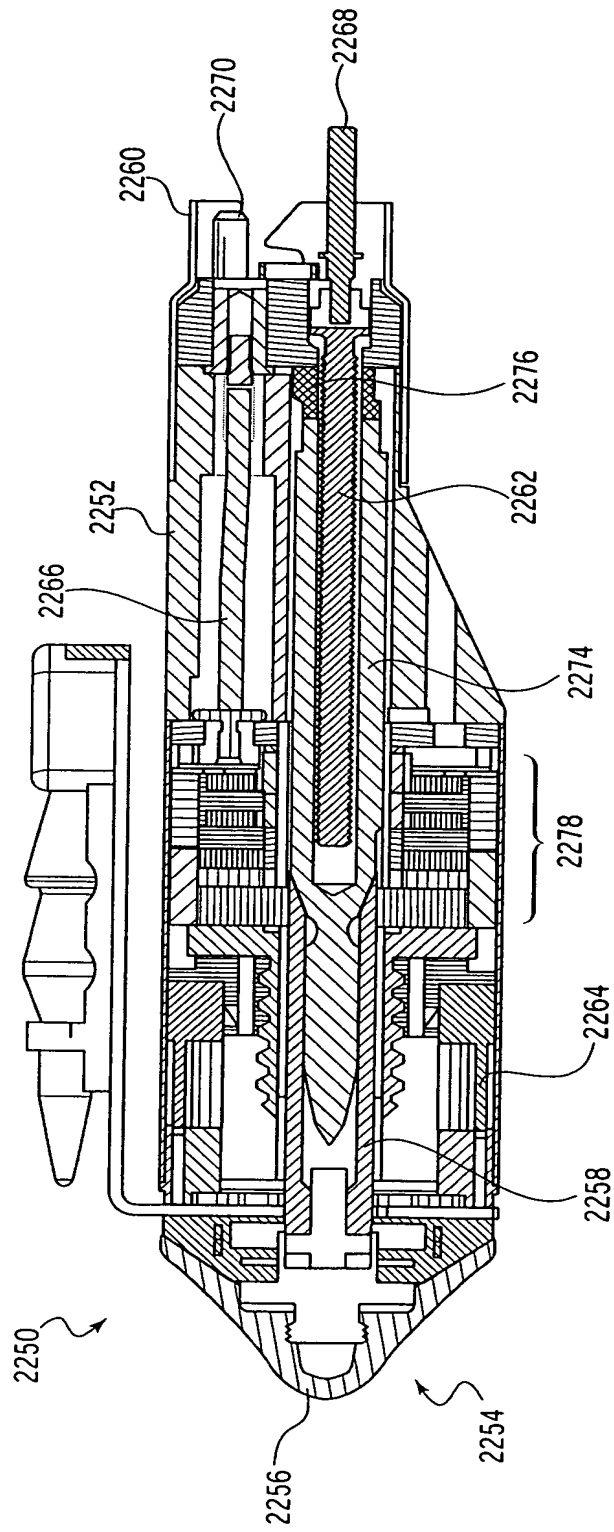


Fig. 9b

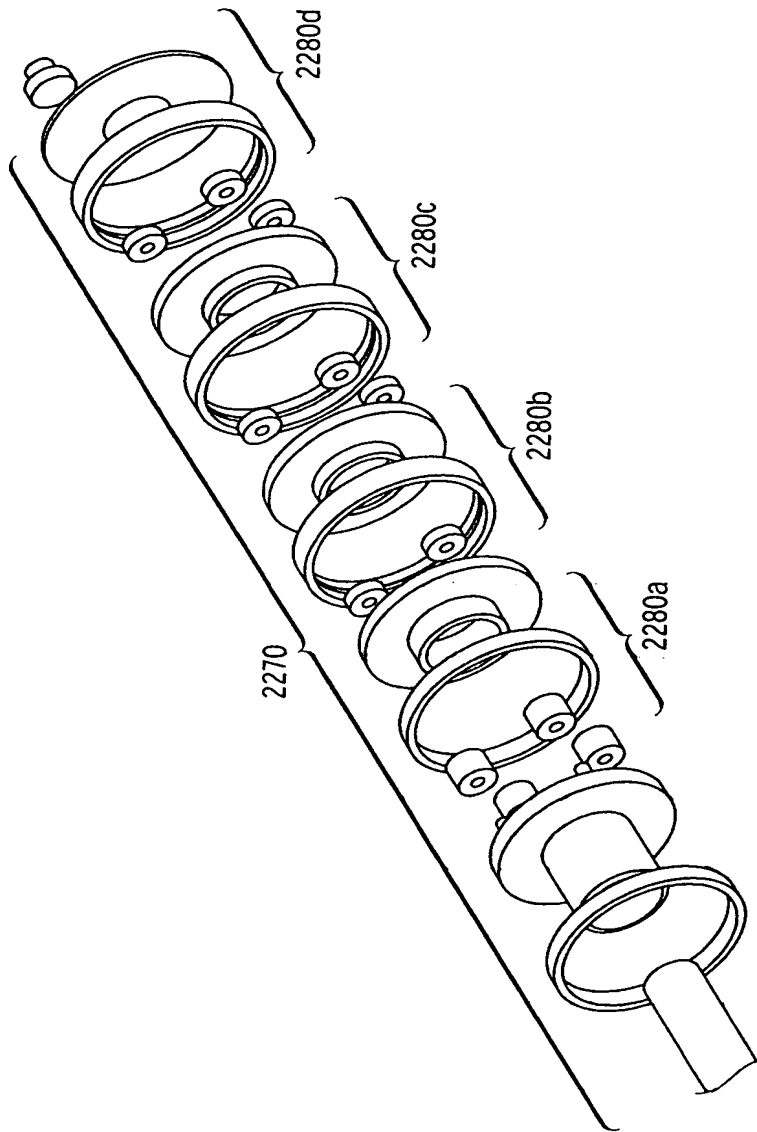


Fig. 9c

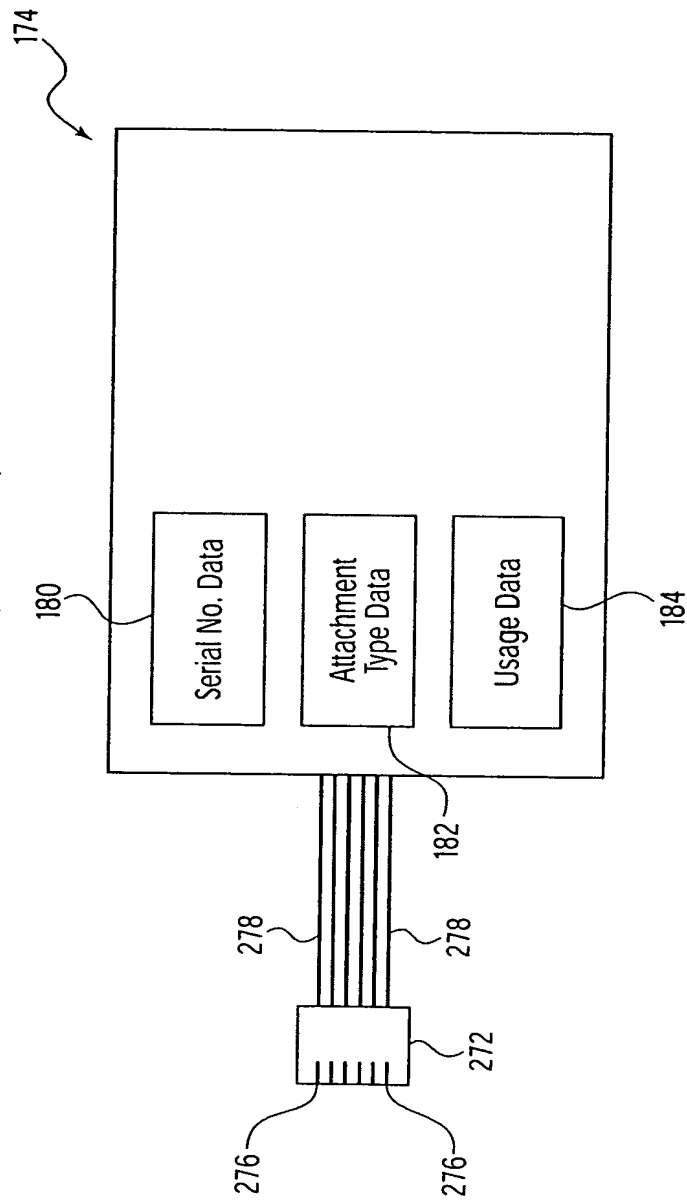


Fig. 10

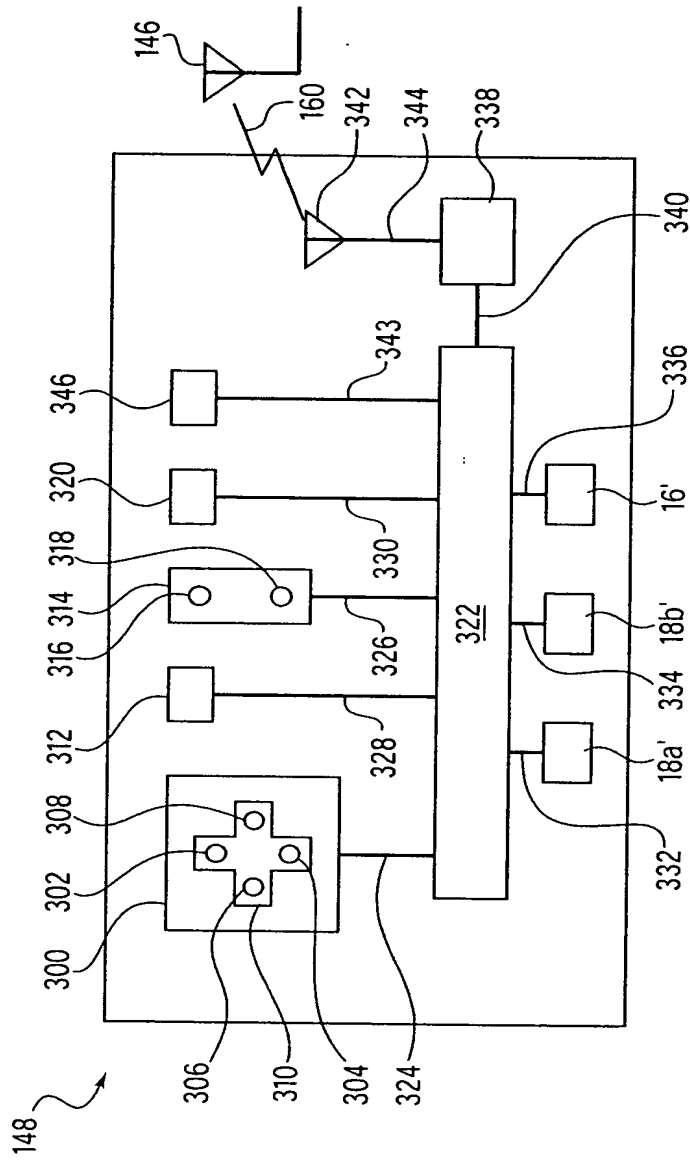
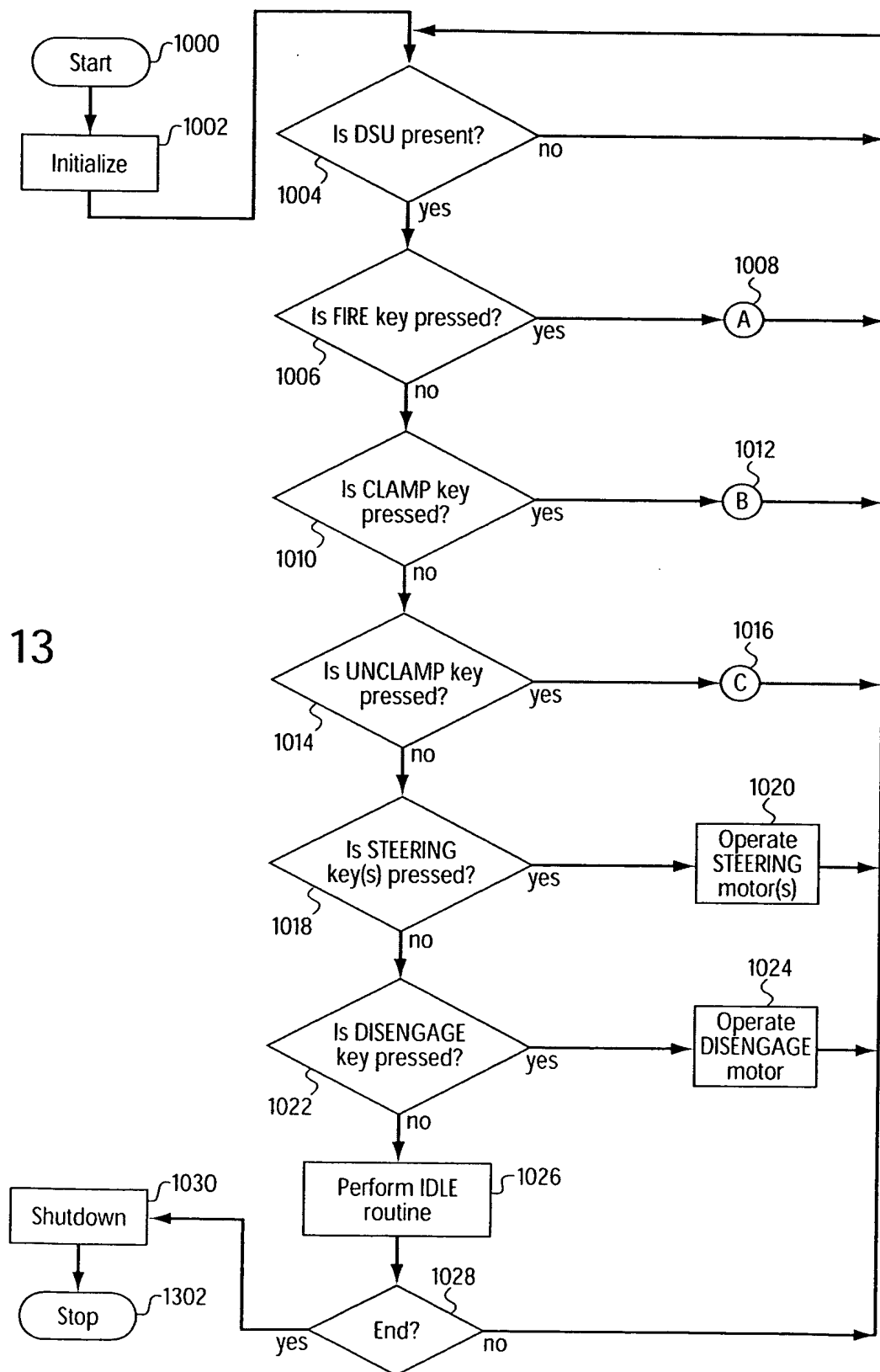


Fig. 11

Fig. 13



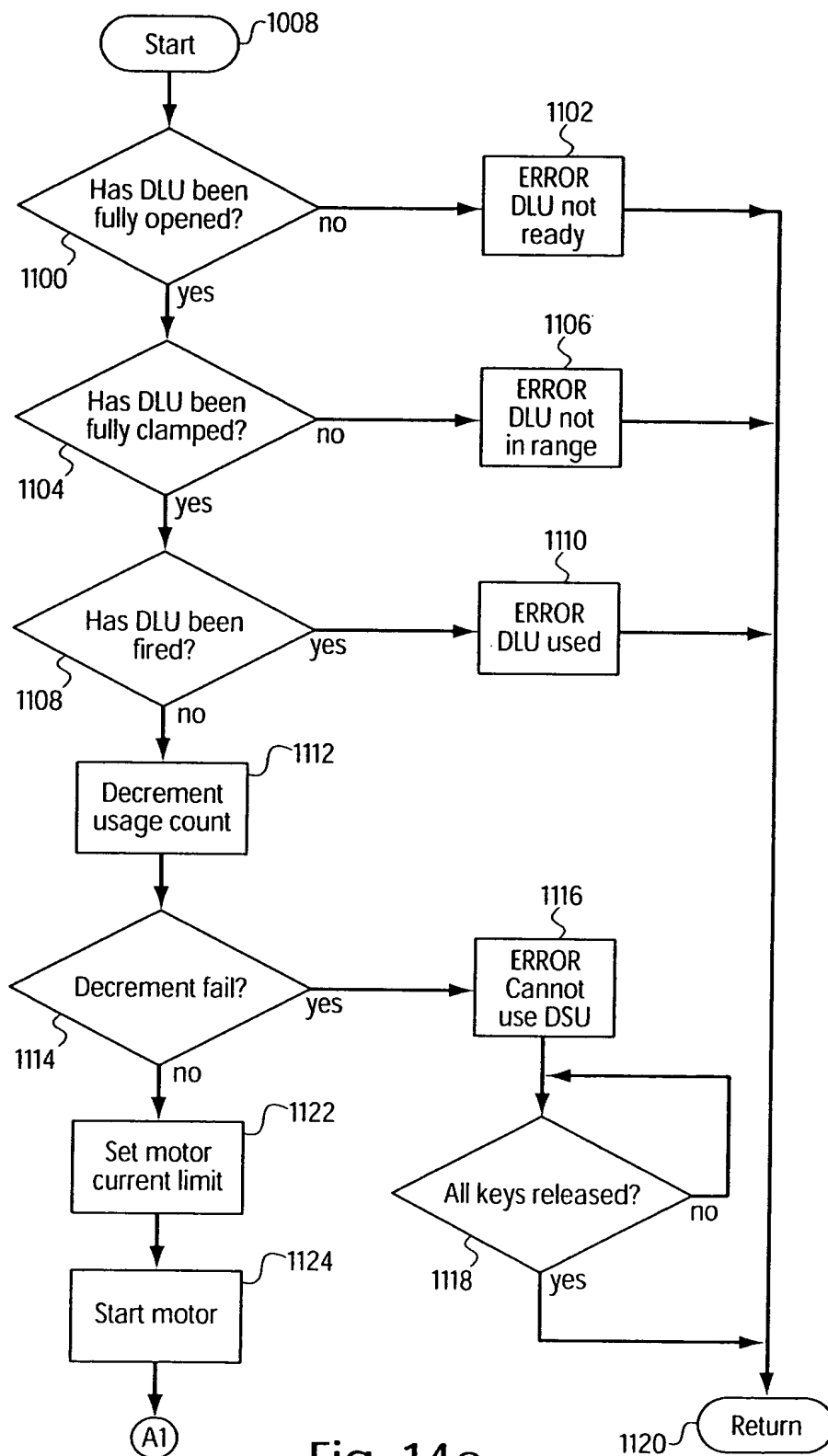


Fig. 14a

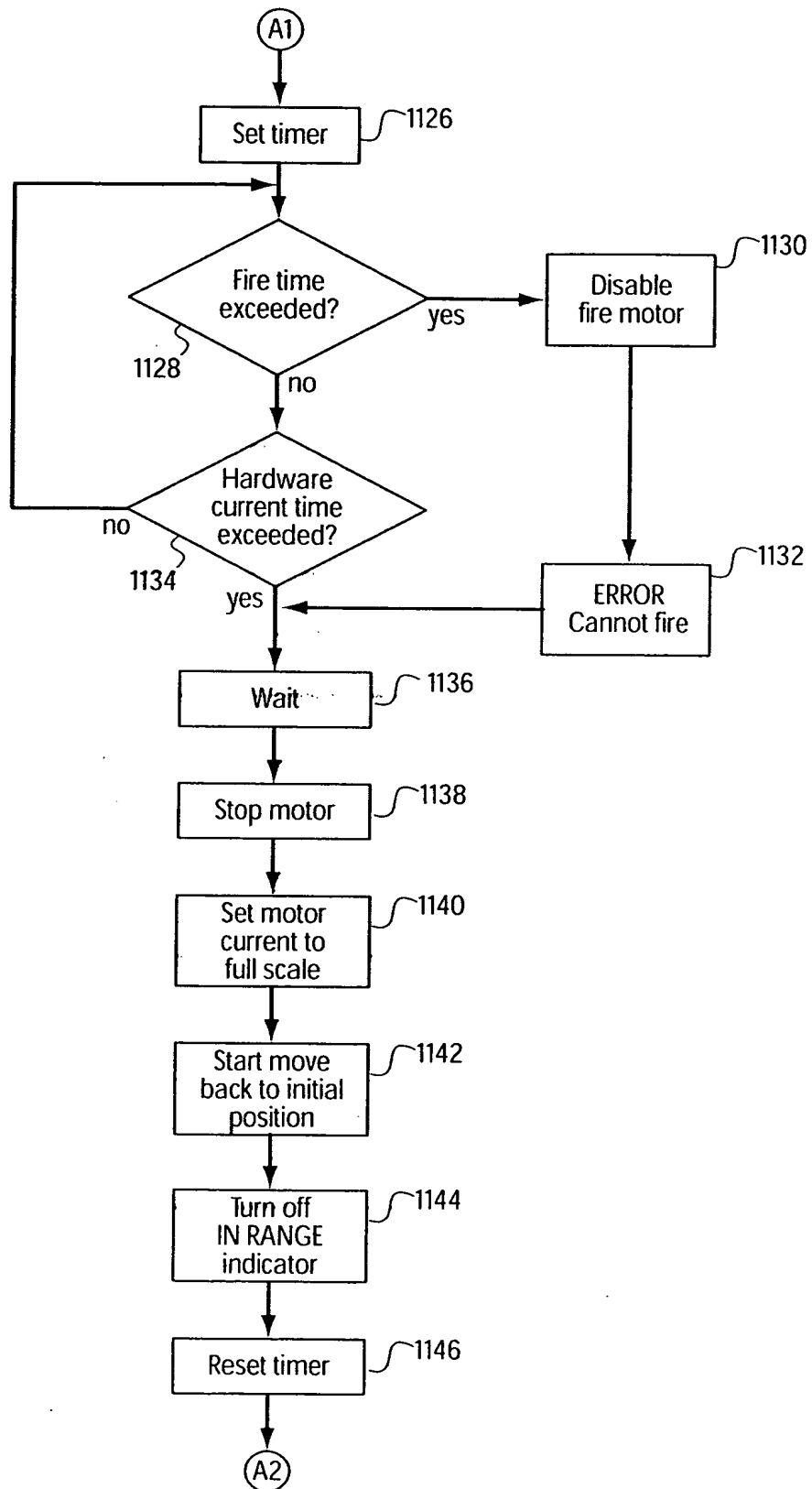


Fig. 14b

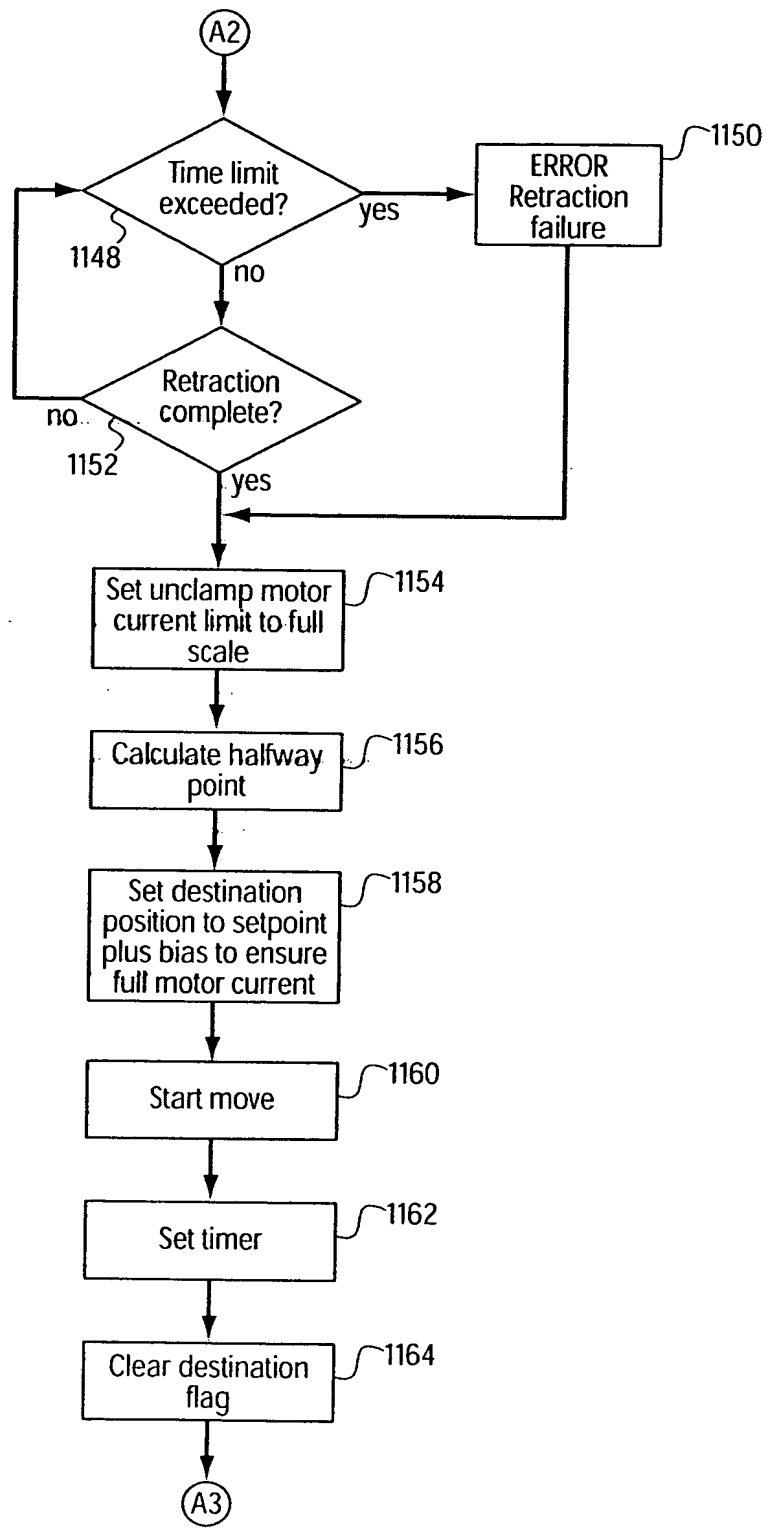


Fig. 14c

Fig. 14d

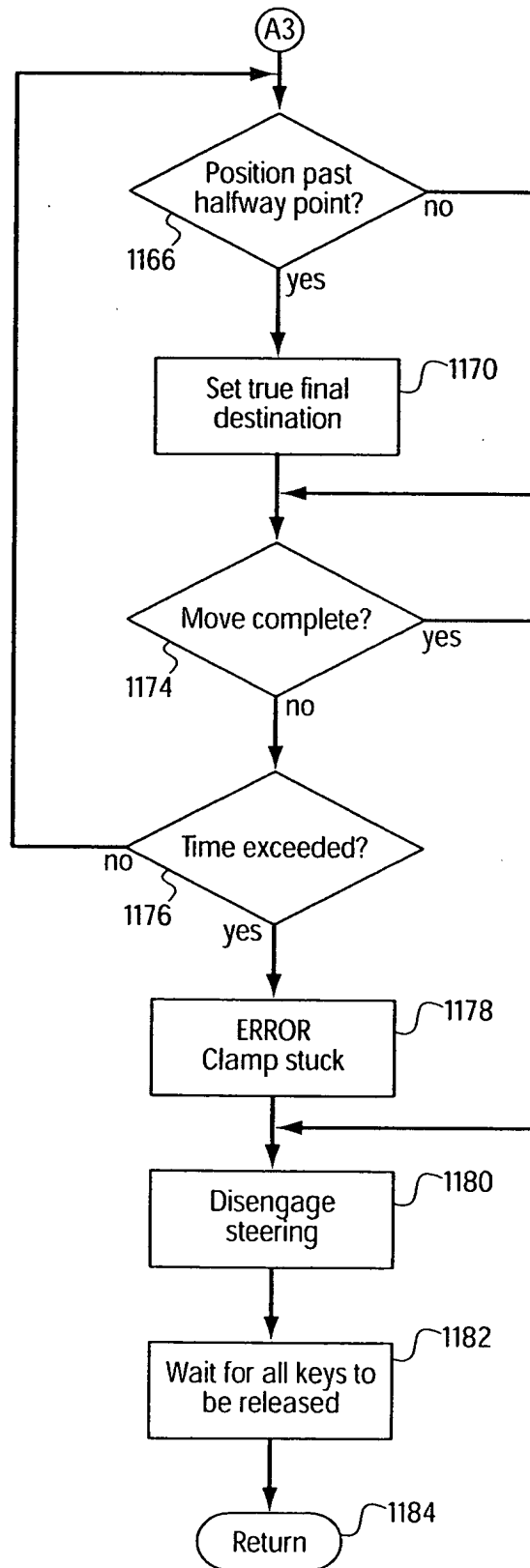


Fig.15a

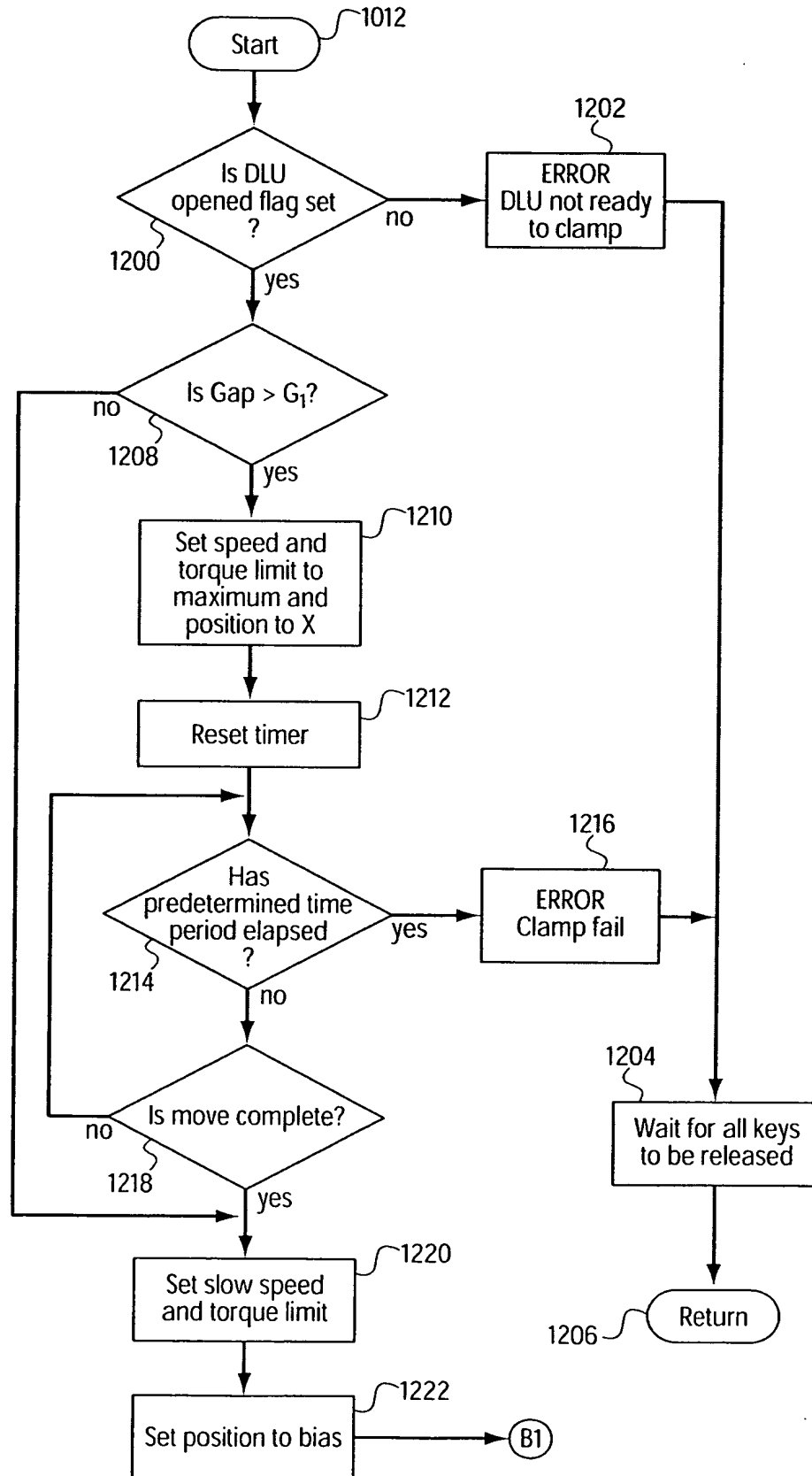


Fig.15b

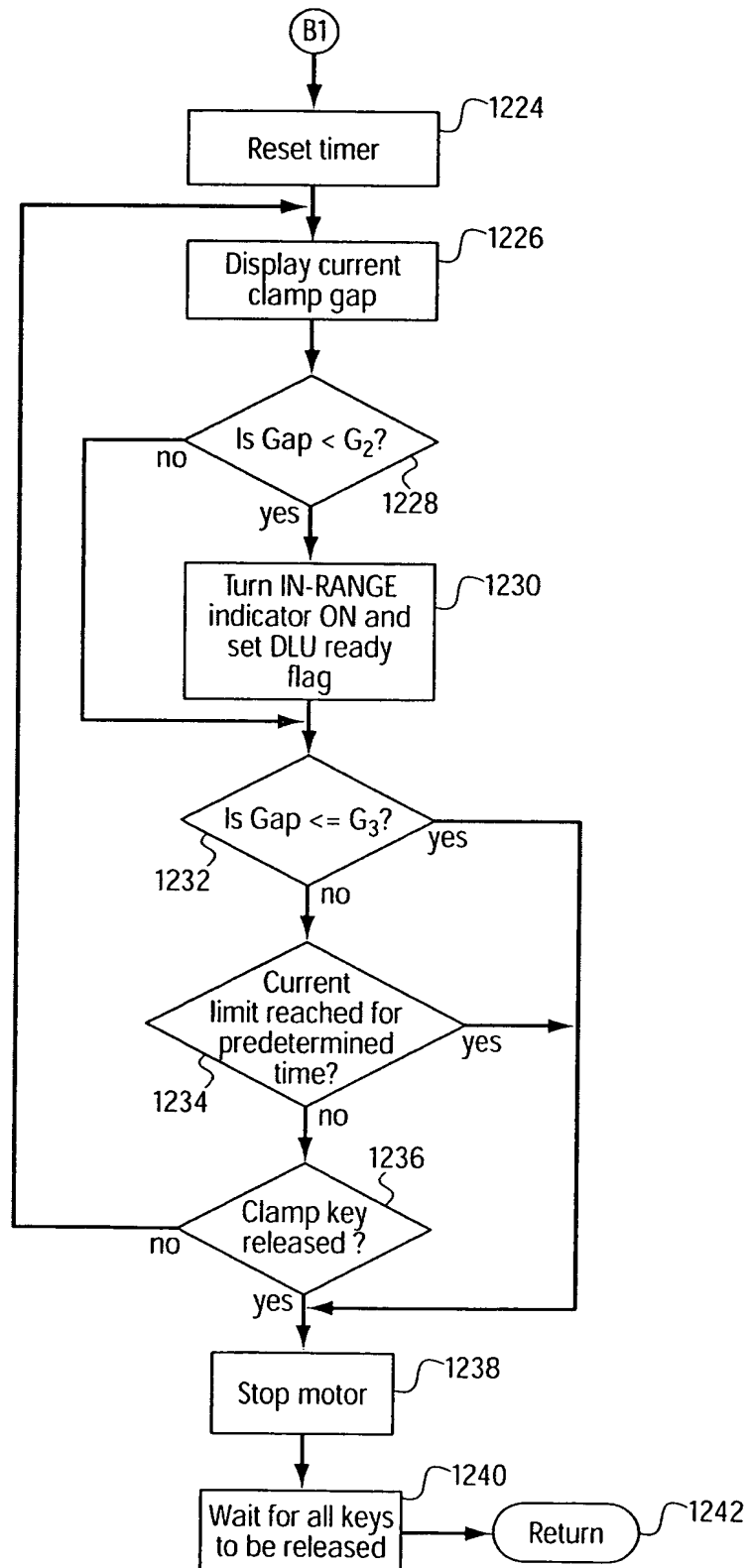
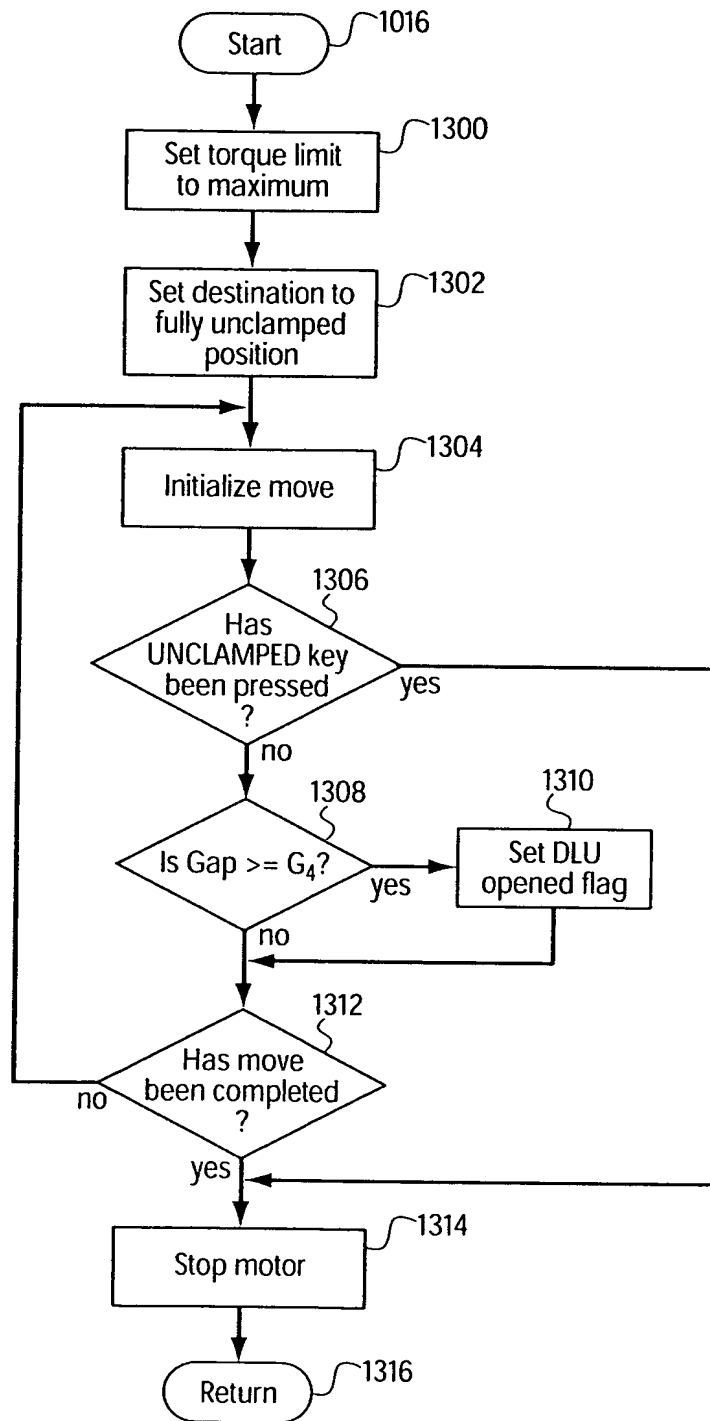


Fig.16



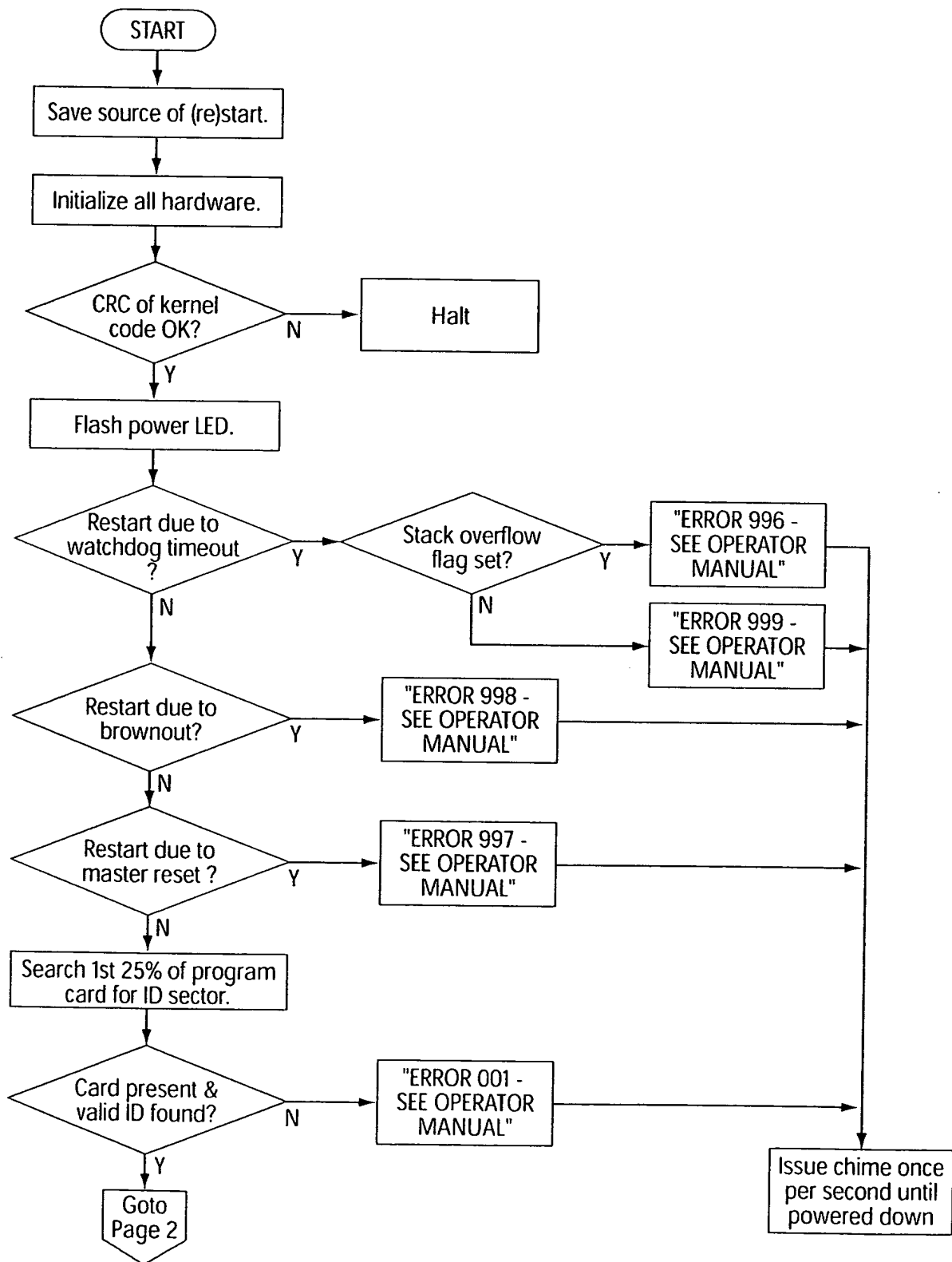


Fig. 17a

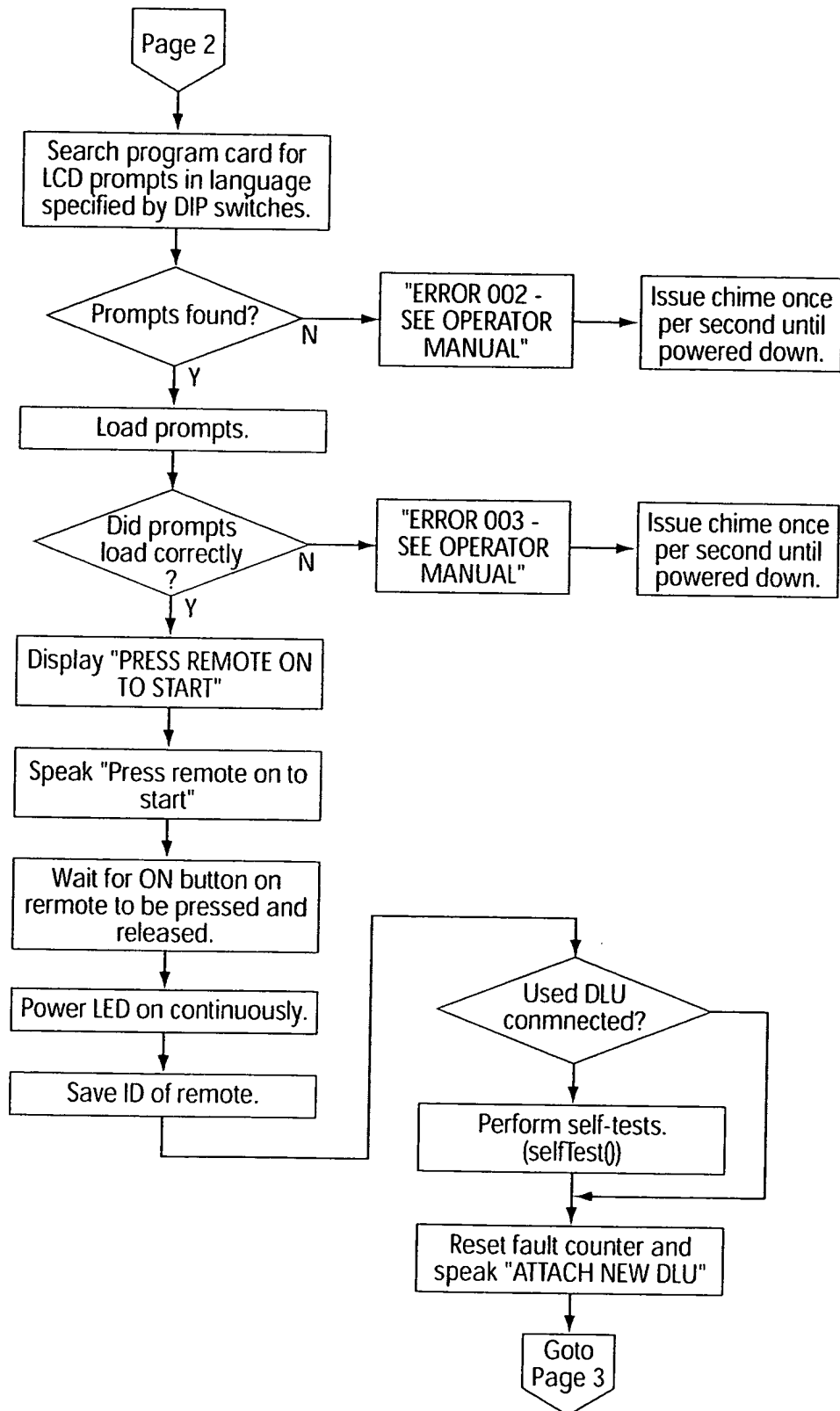


Fig. 17b

Main Processing Loop

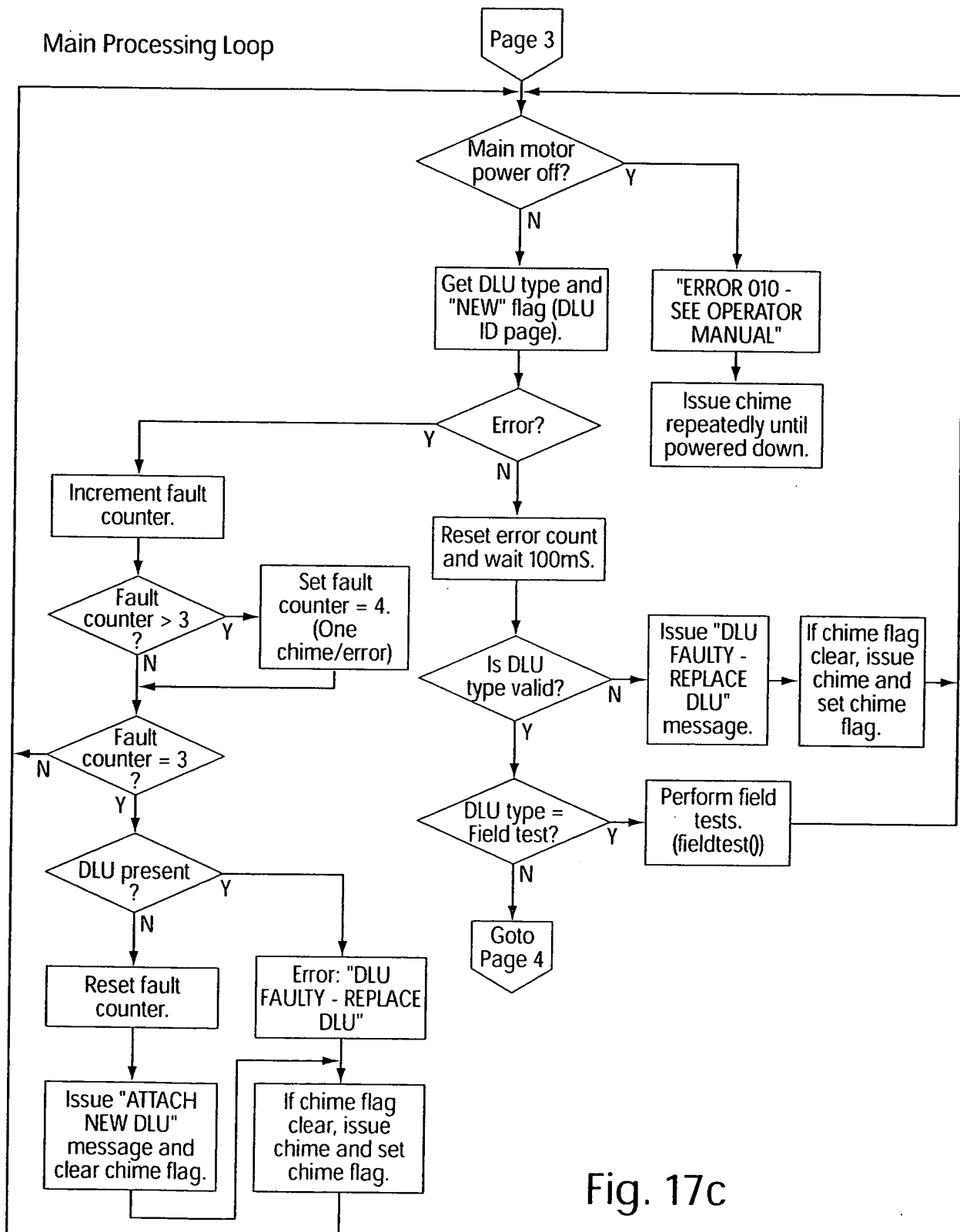


Fig. 17c

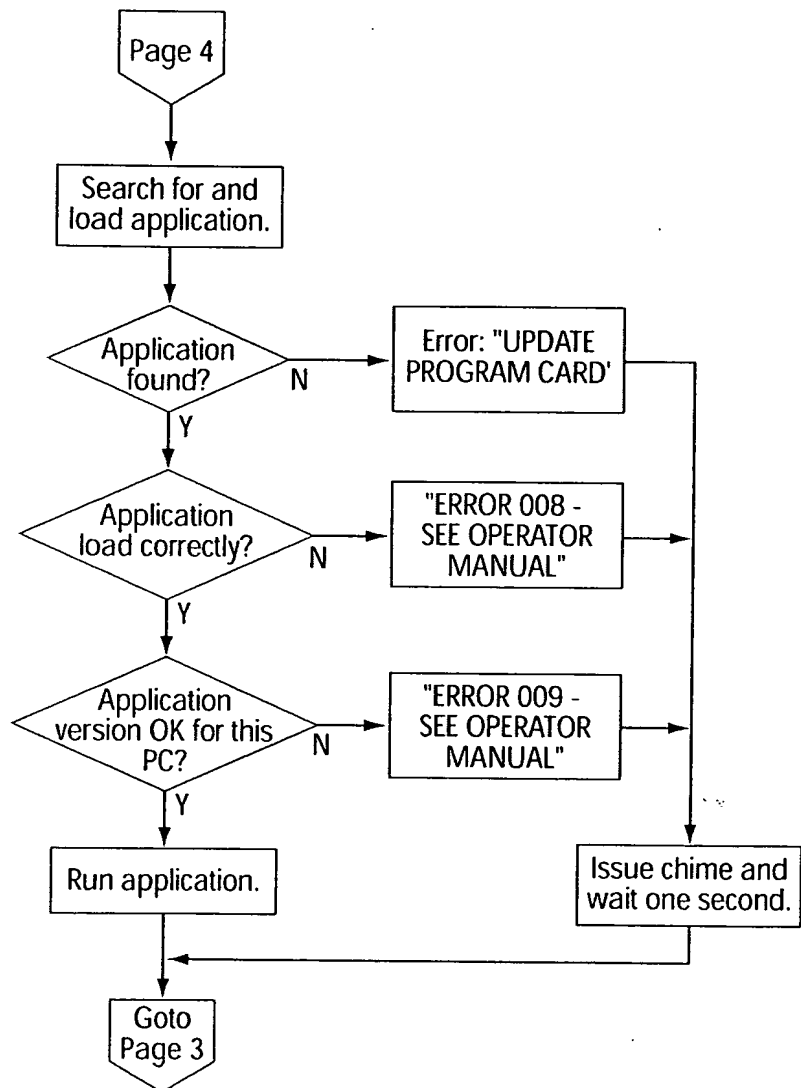


Fig. 17d

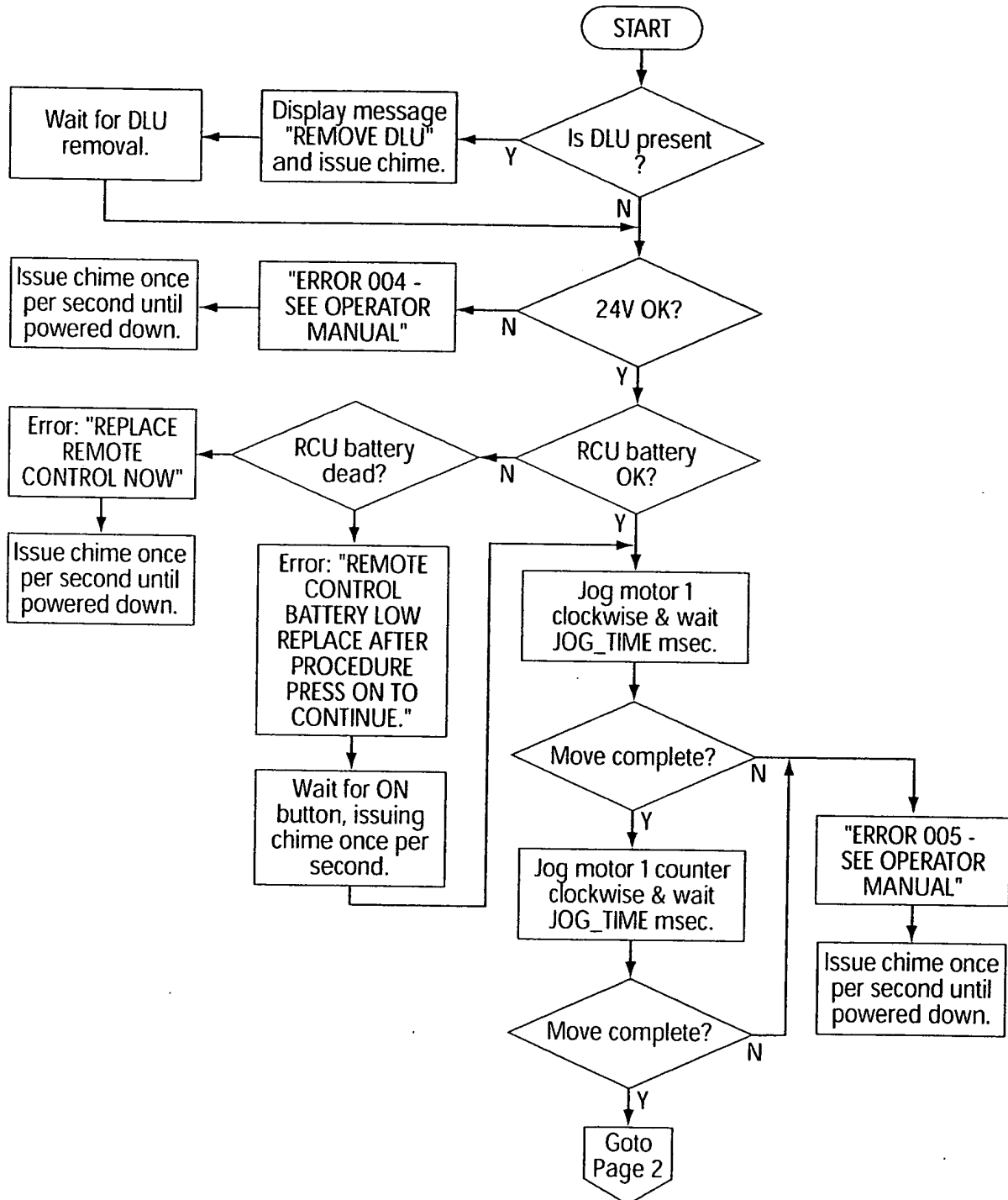


Fig. 18a

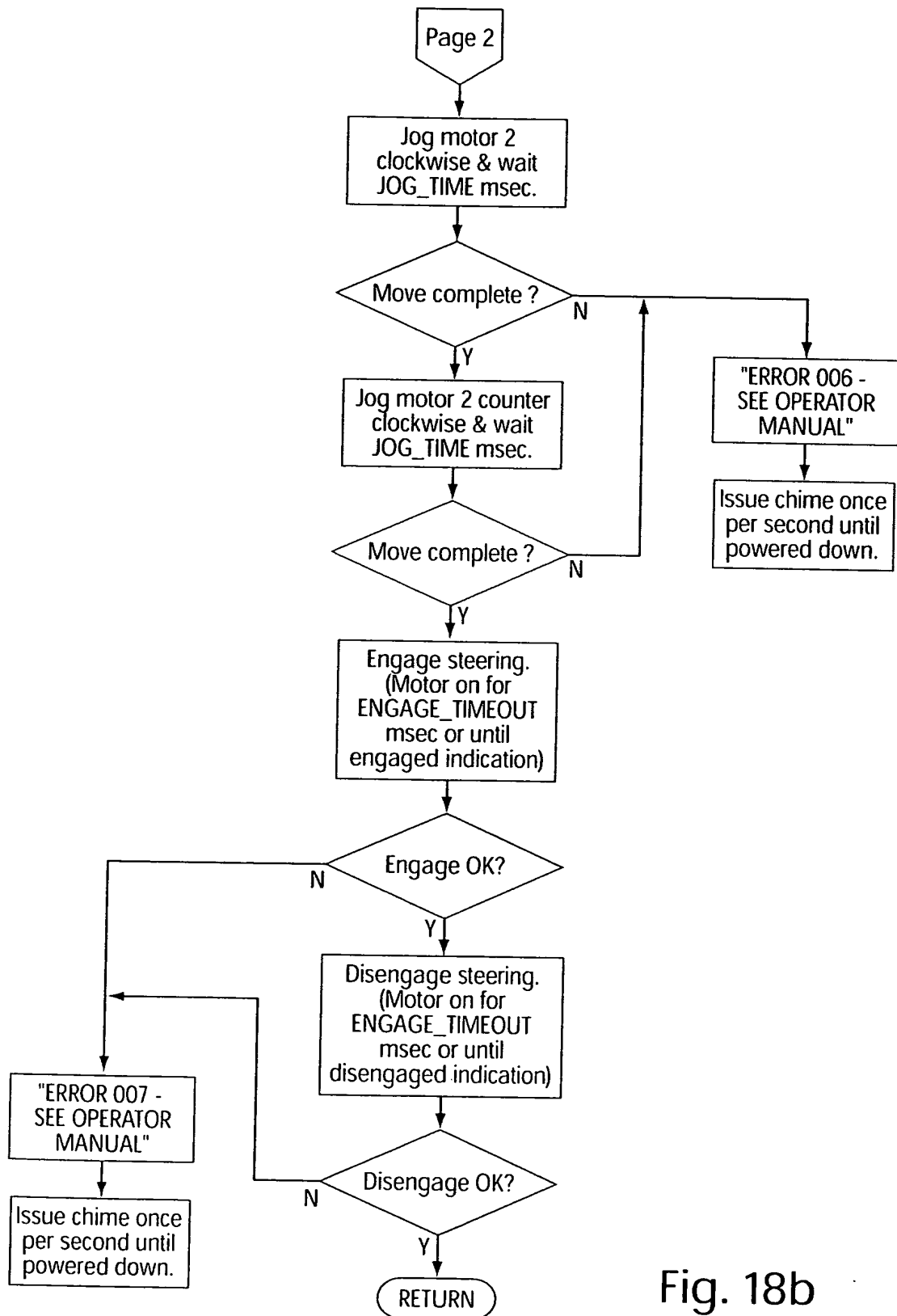


Fig. 18b

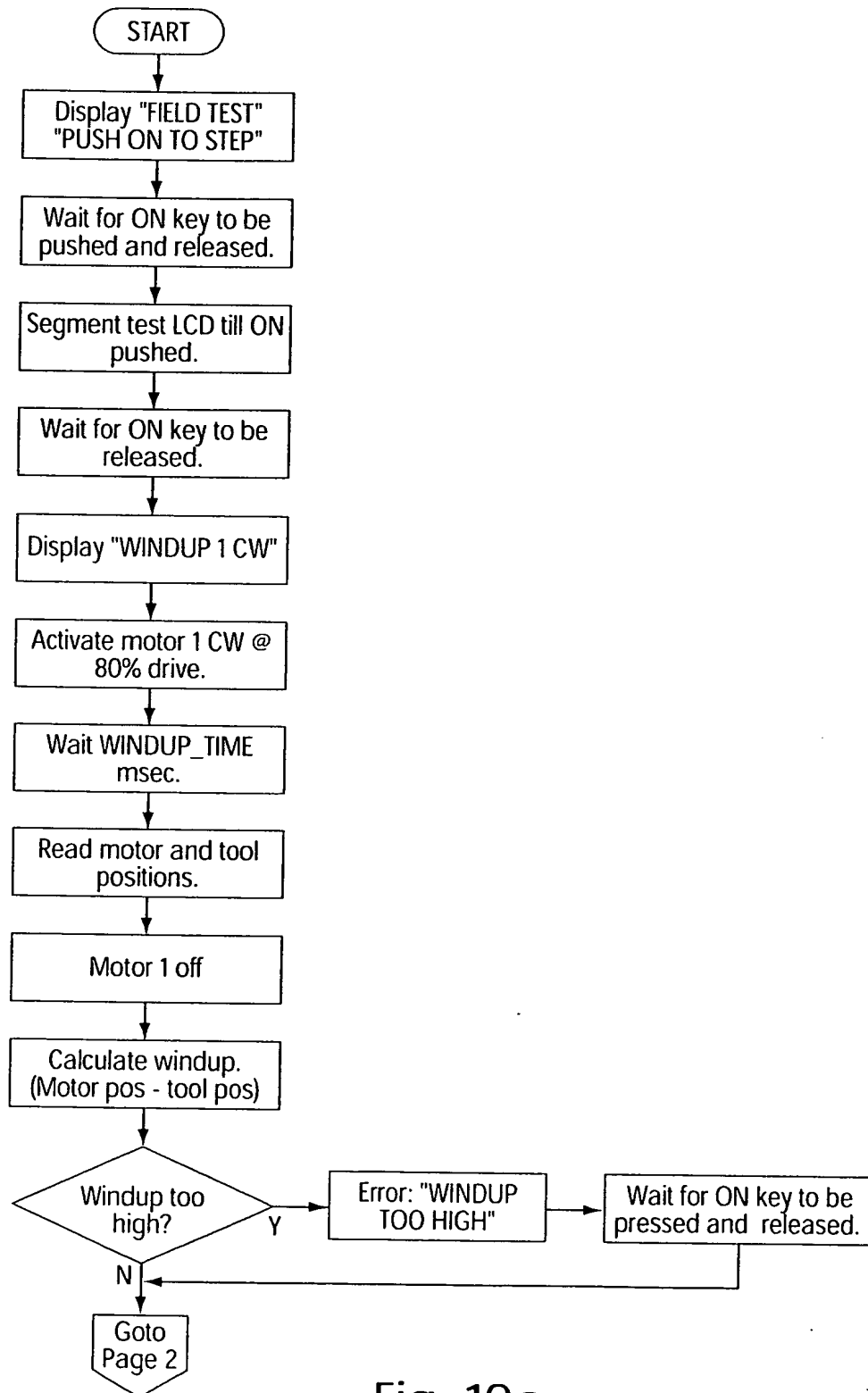


Fig. 19a

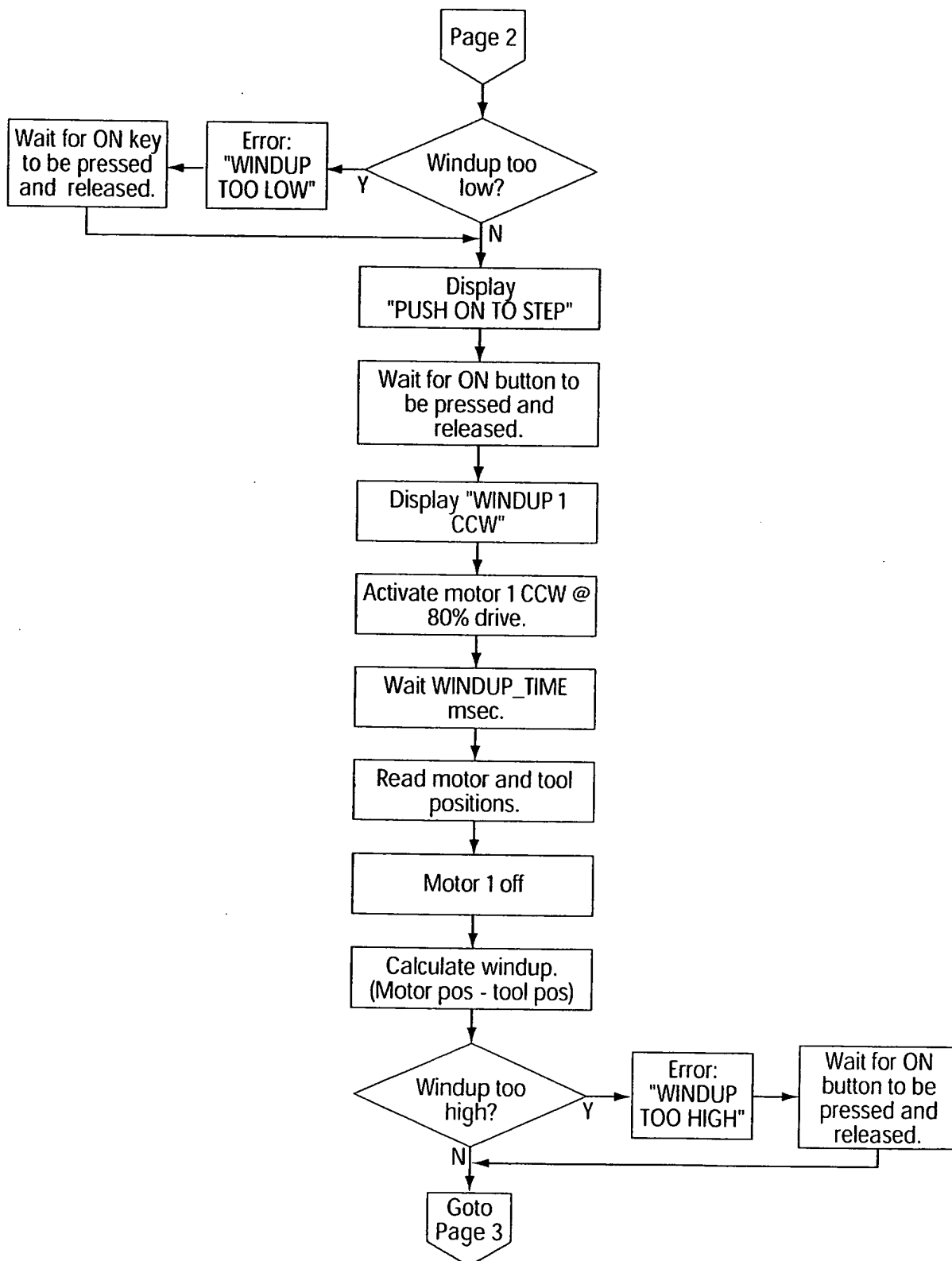


Fig. 19b

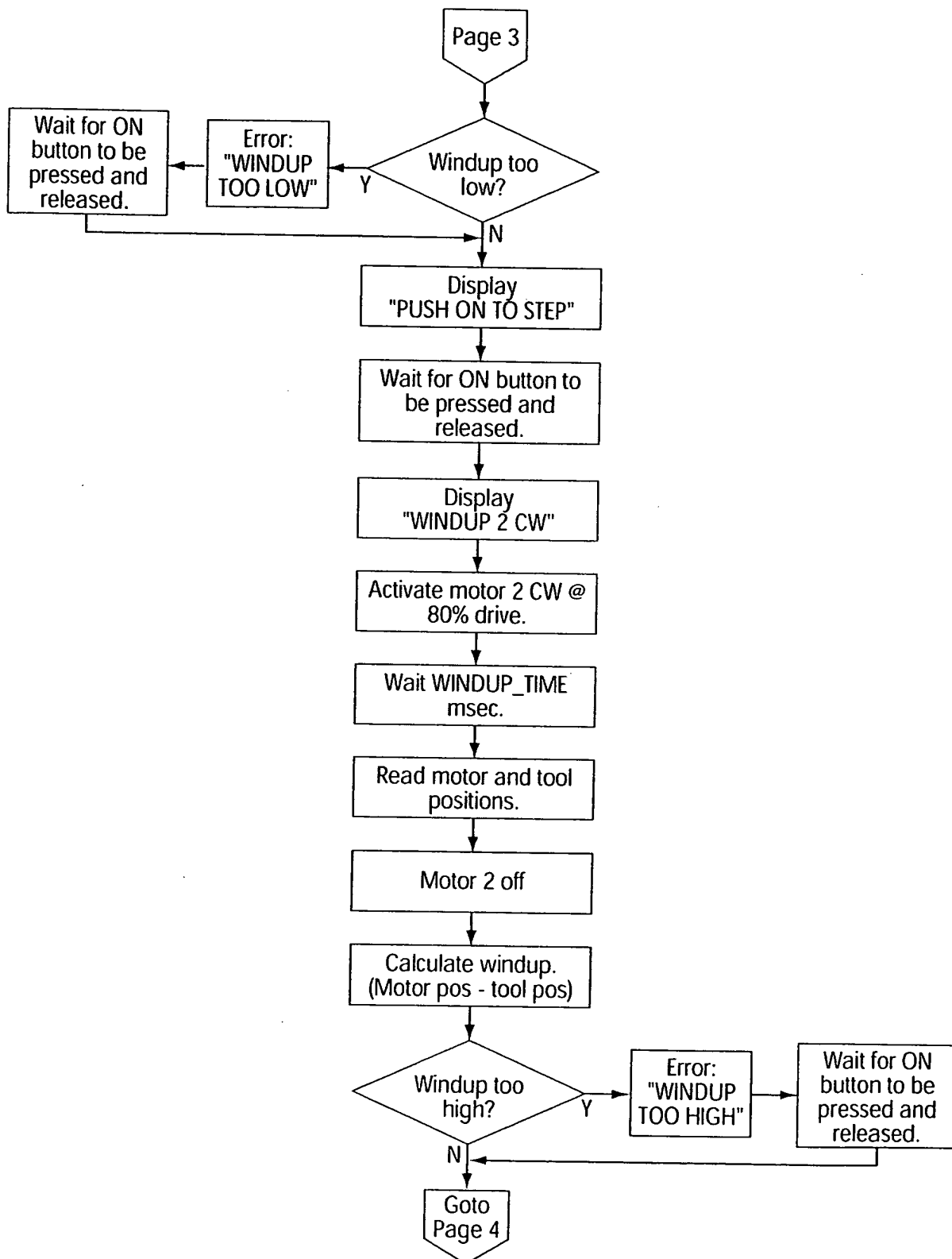


Fig. 19c

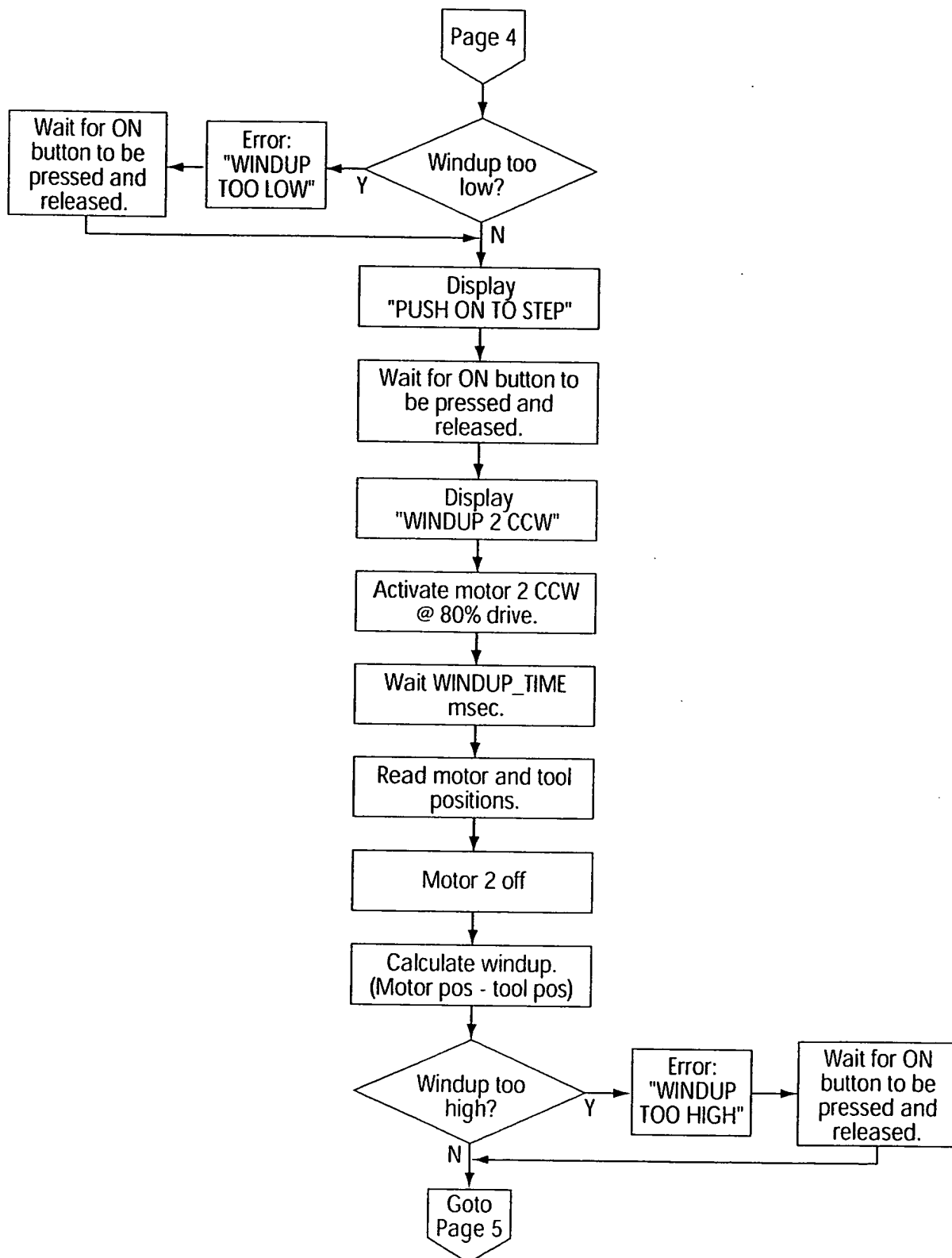


Fig. 19d

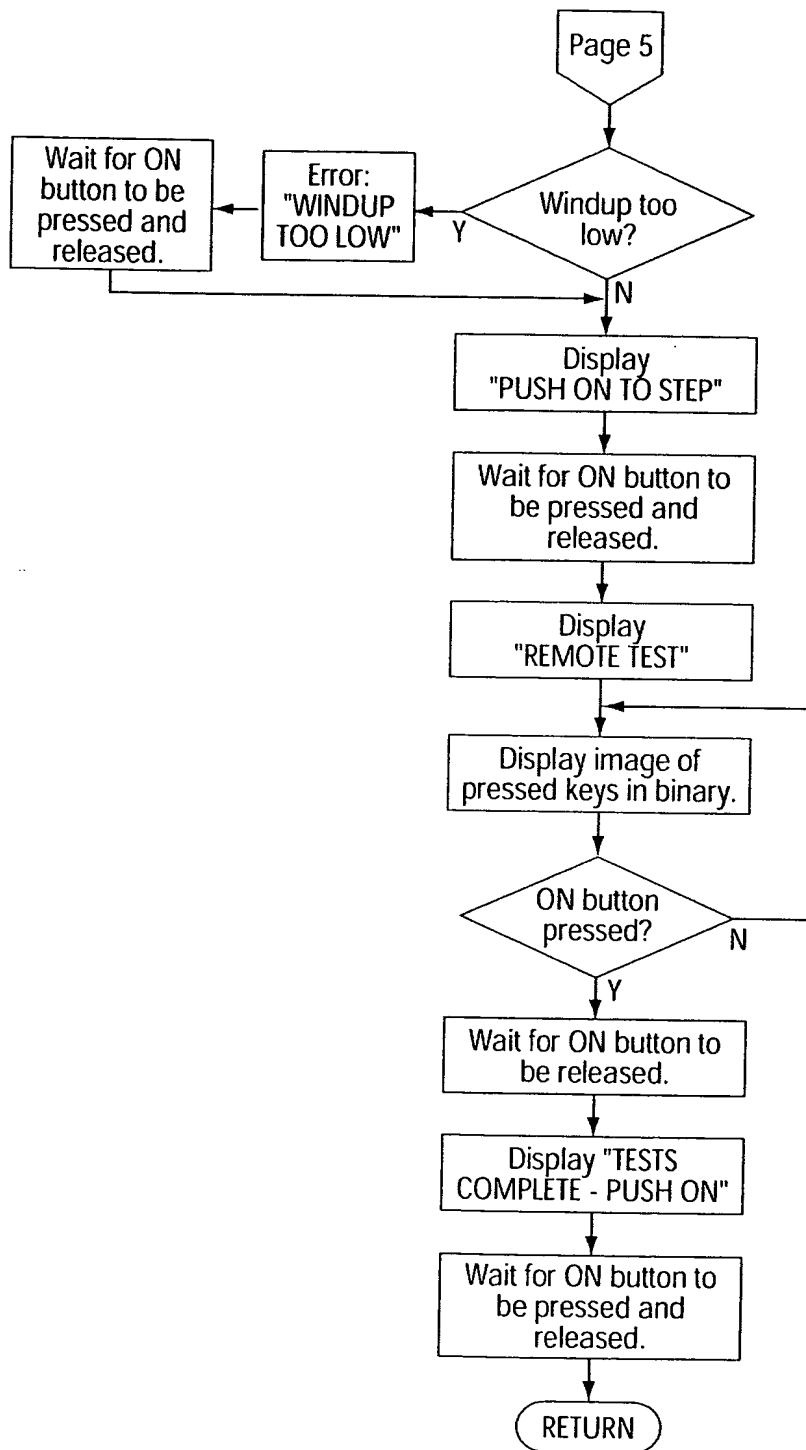


Fig. 19e

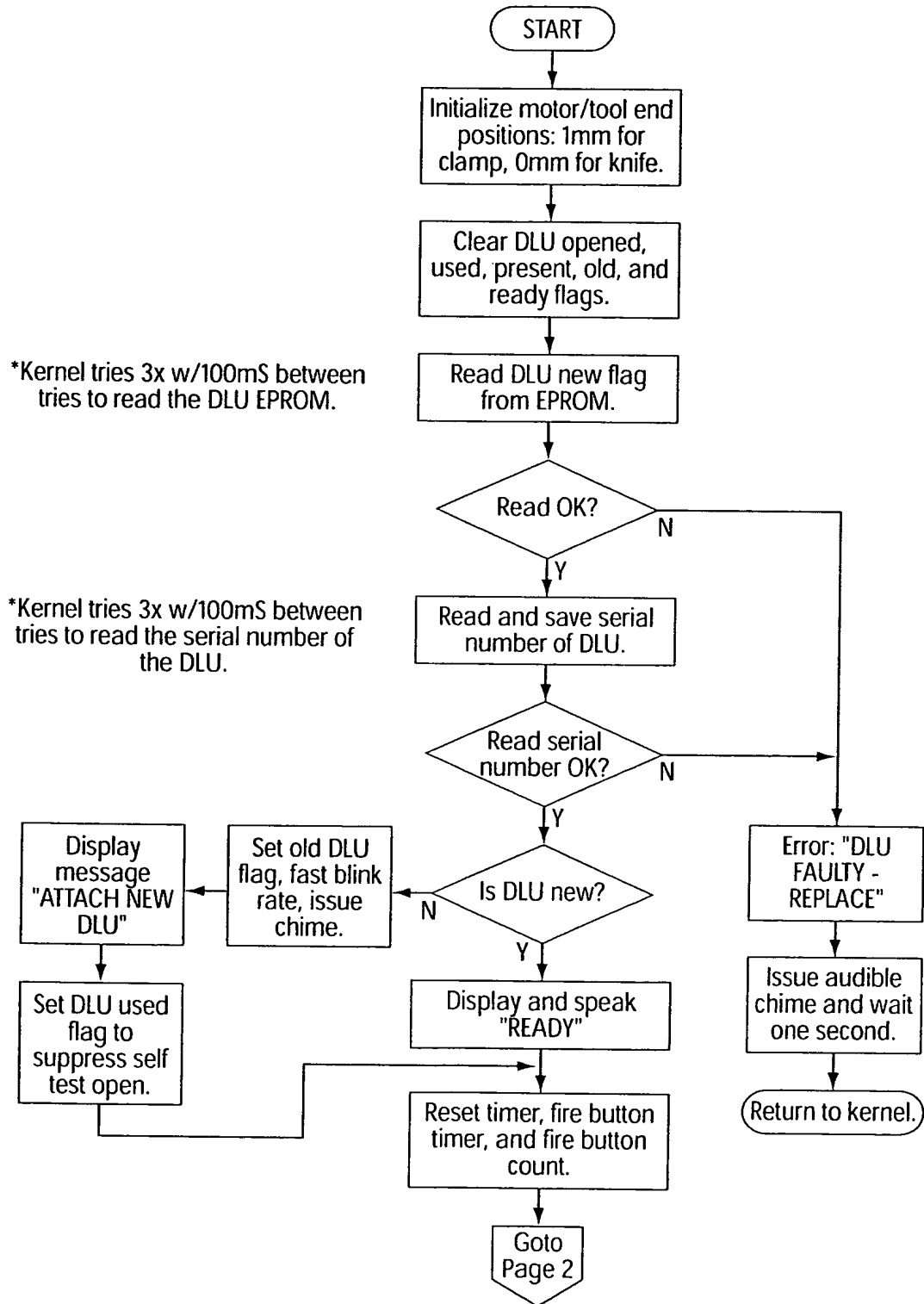


Fig. 20a

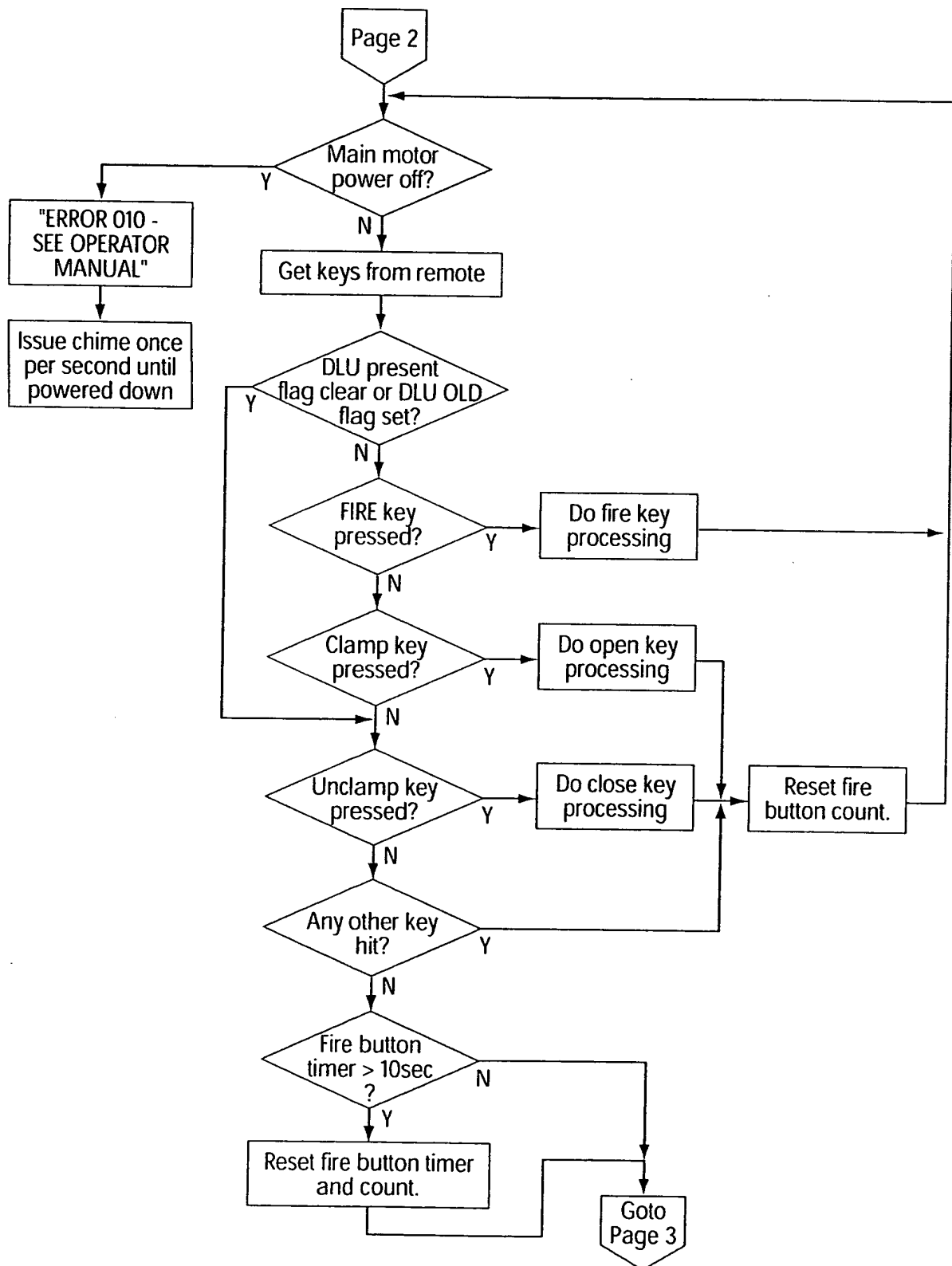


Fig. 20b

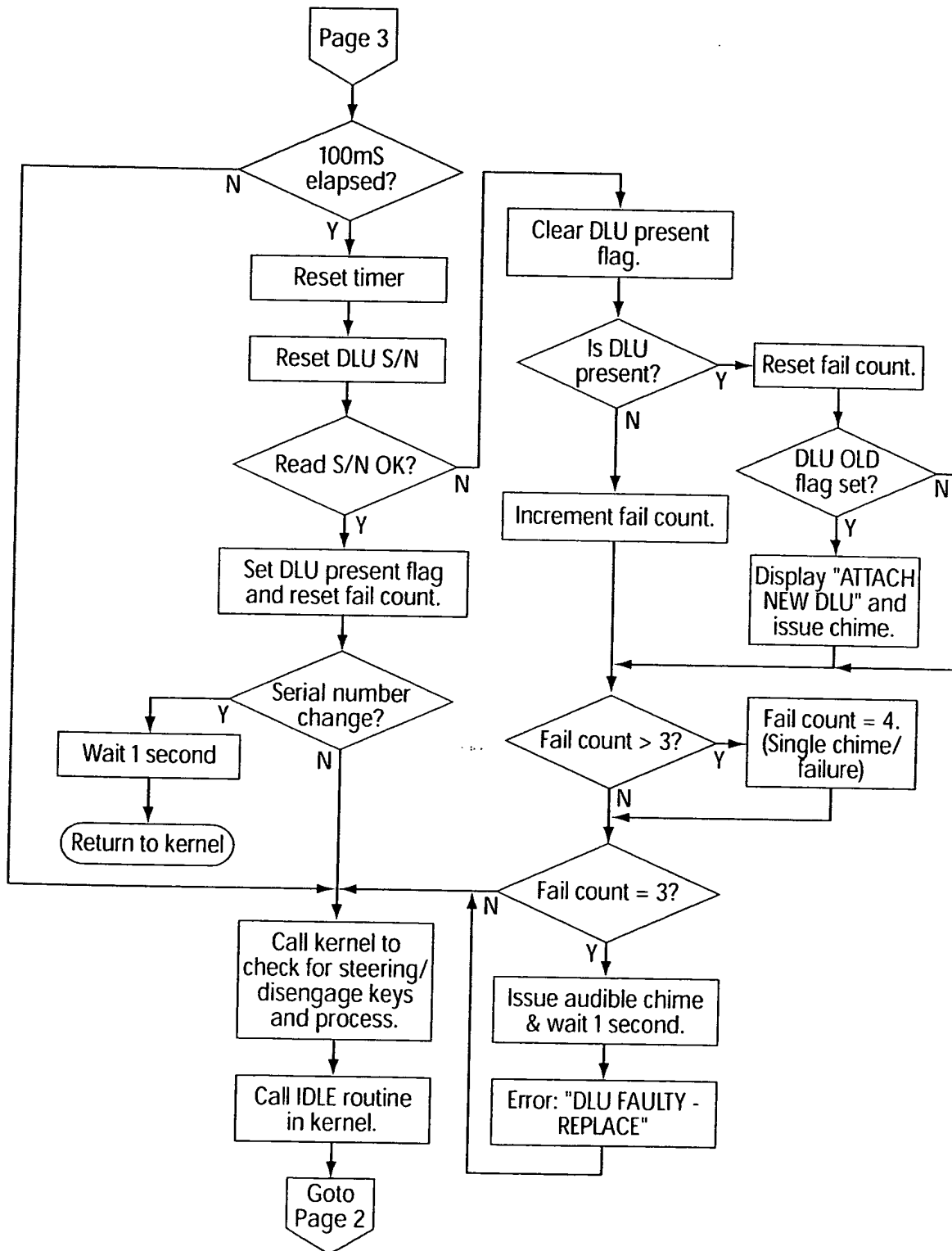
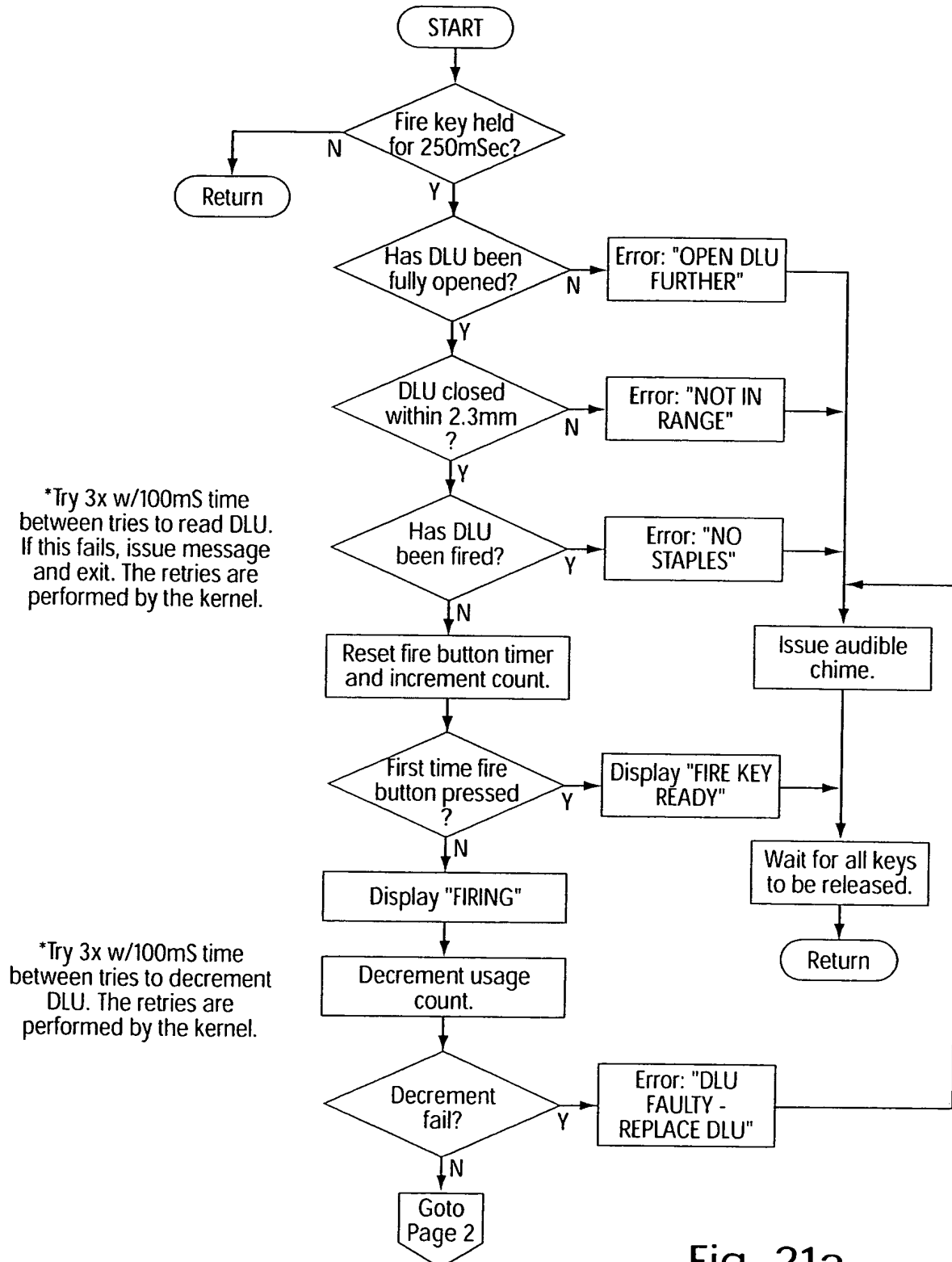
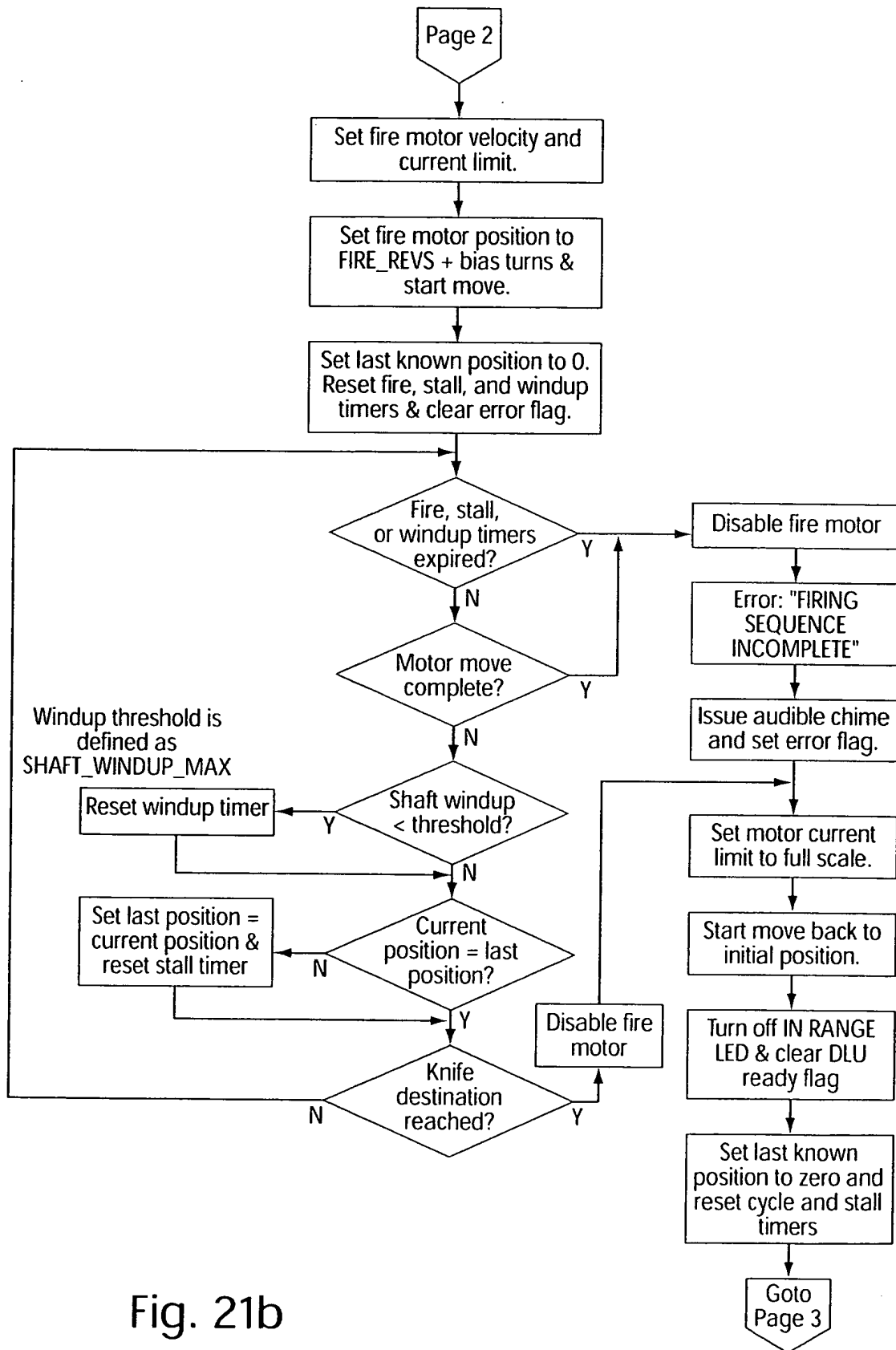


Fig. 20c





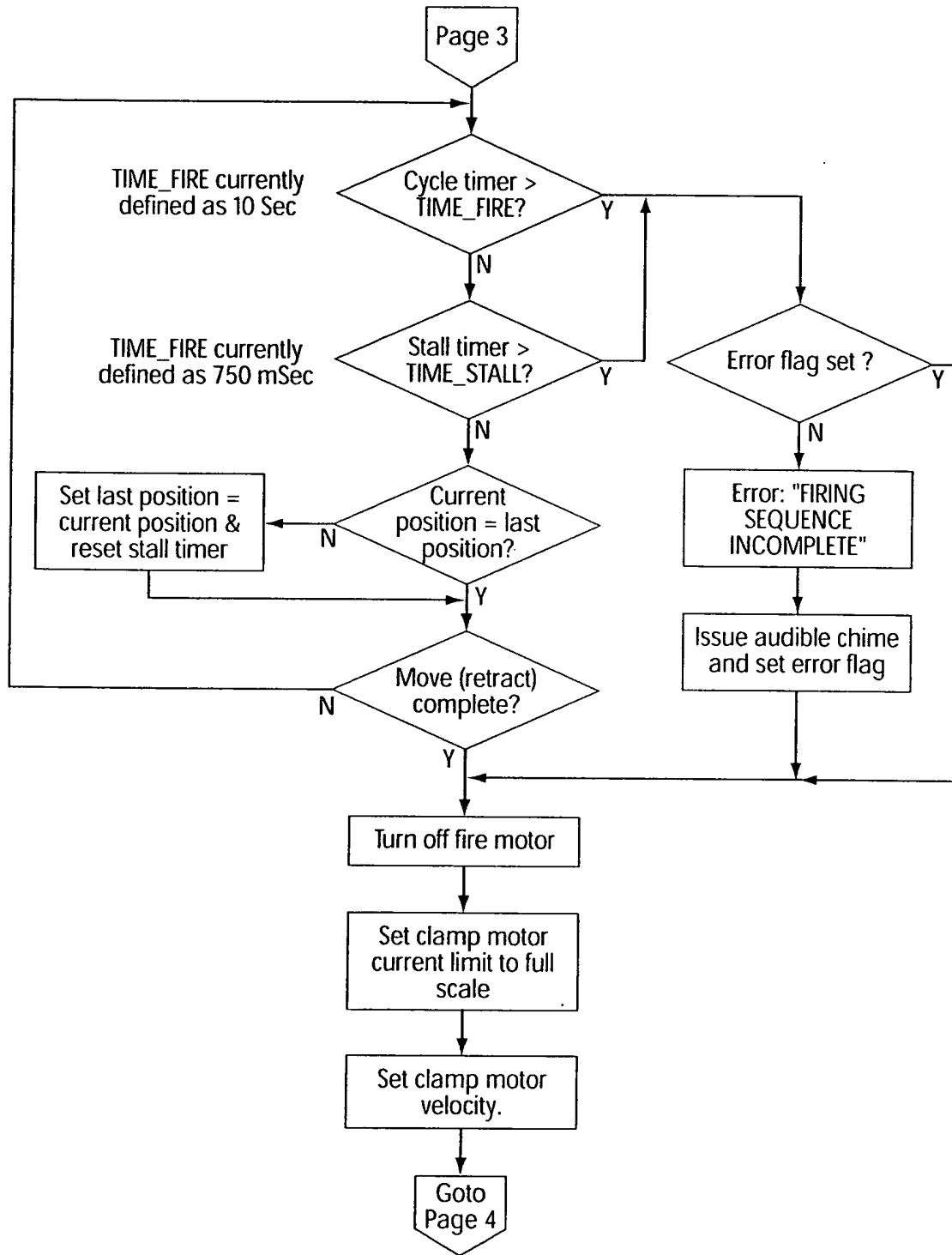


Fig. 21c

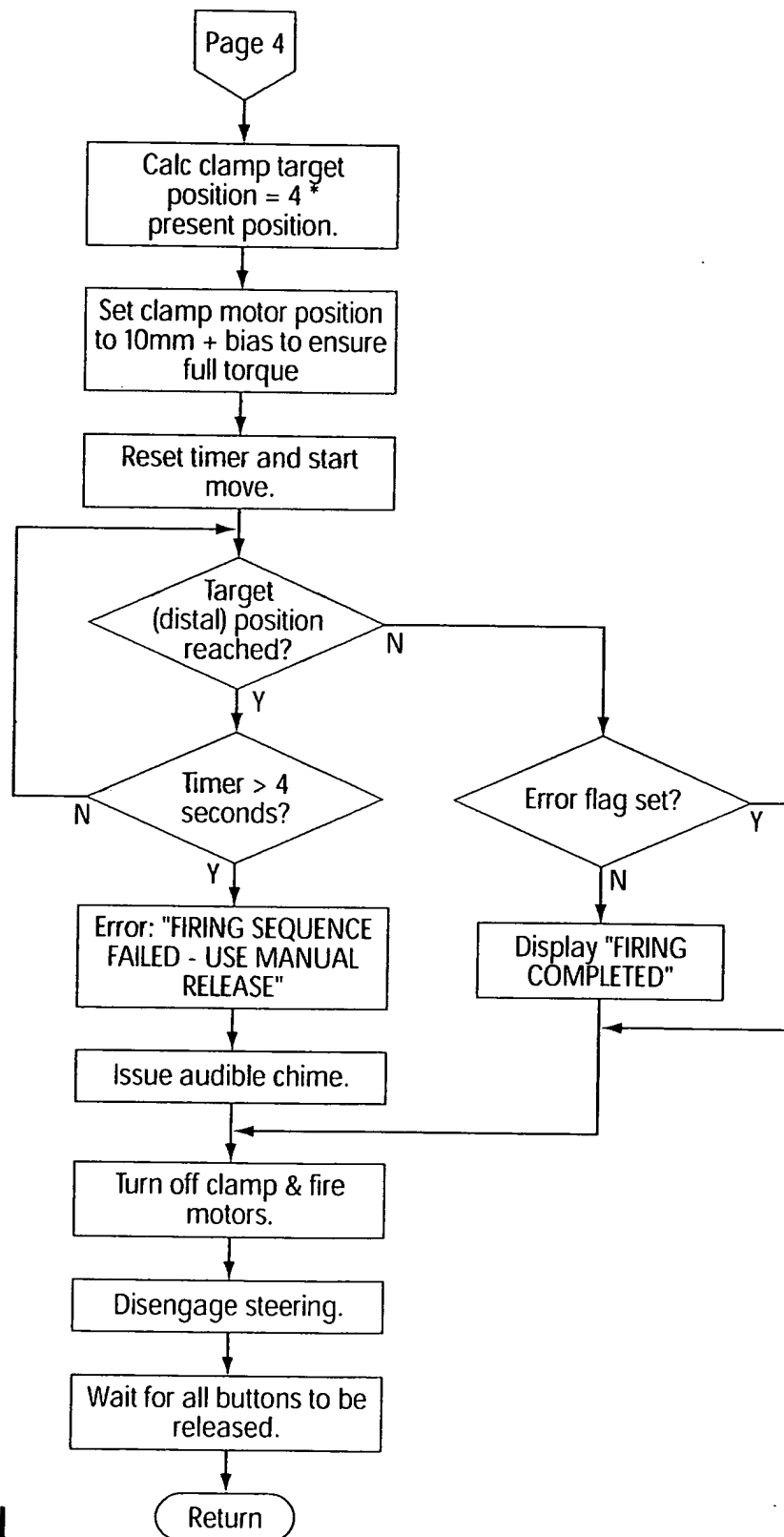


Fig. 21d

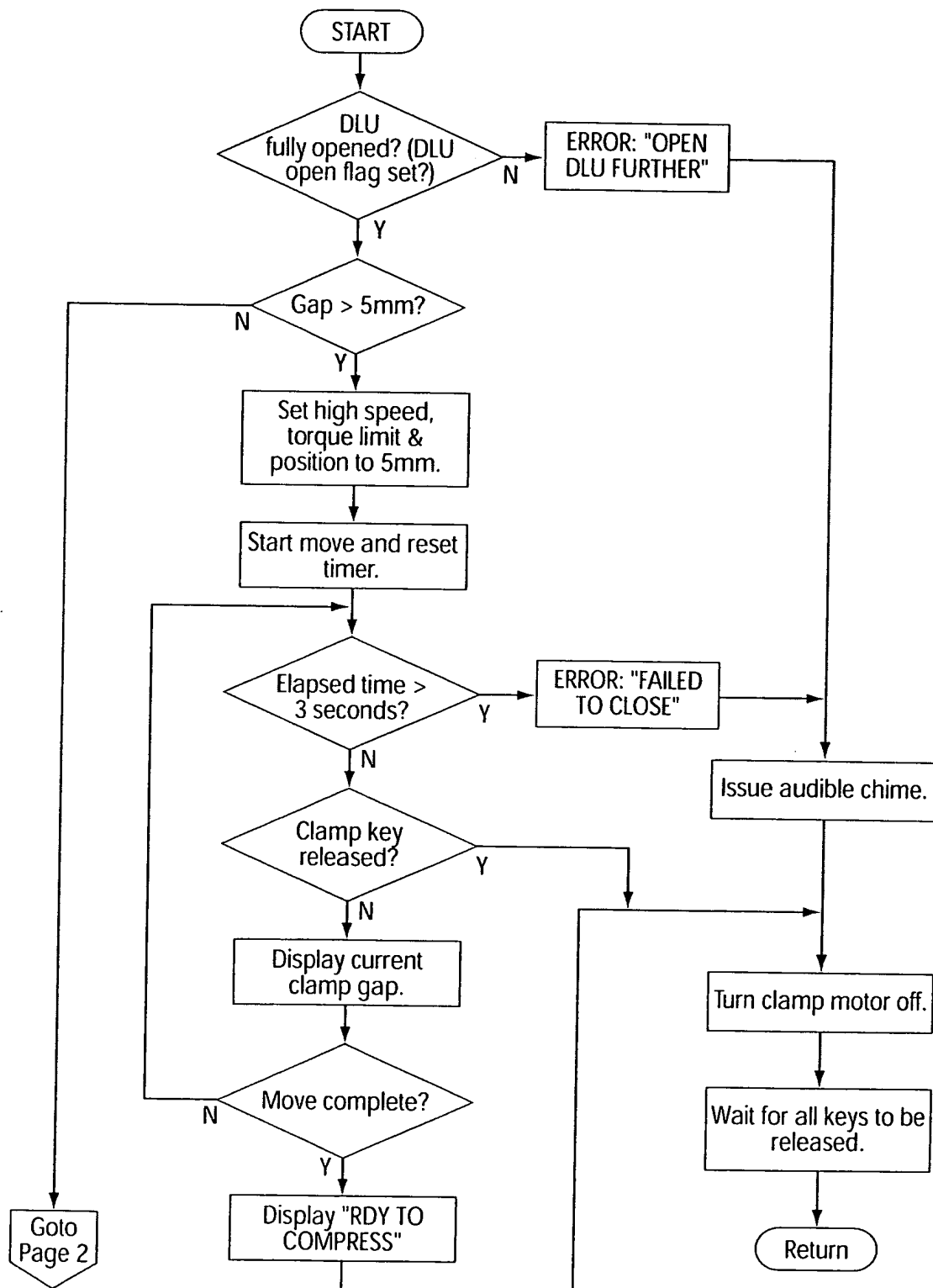


Fig. 22a

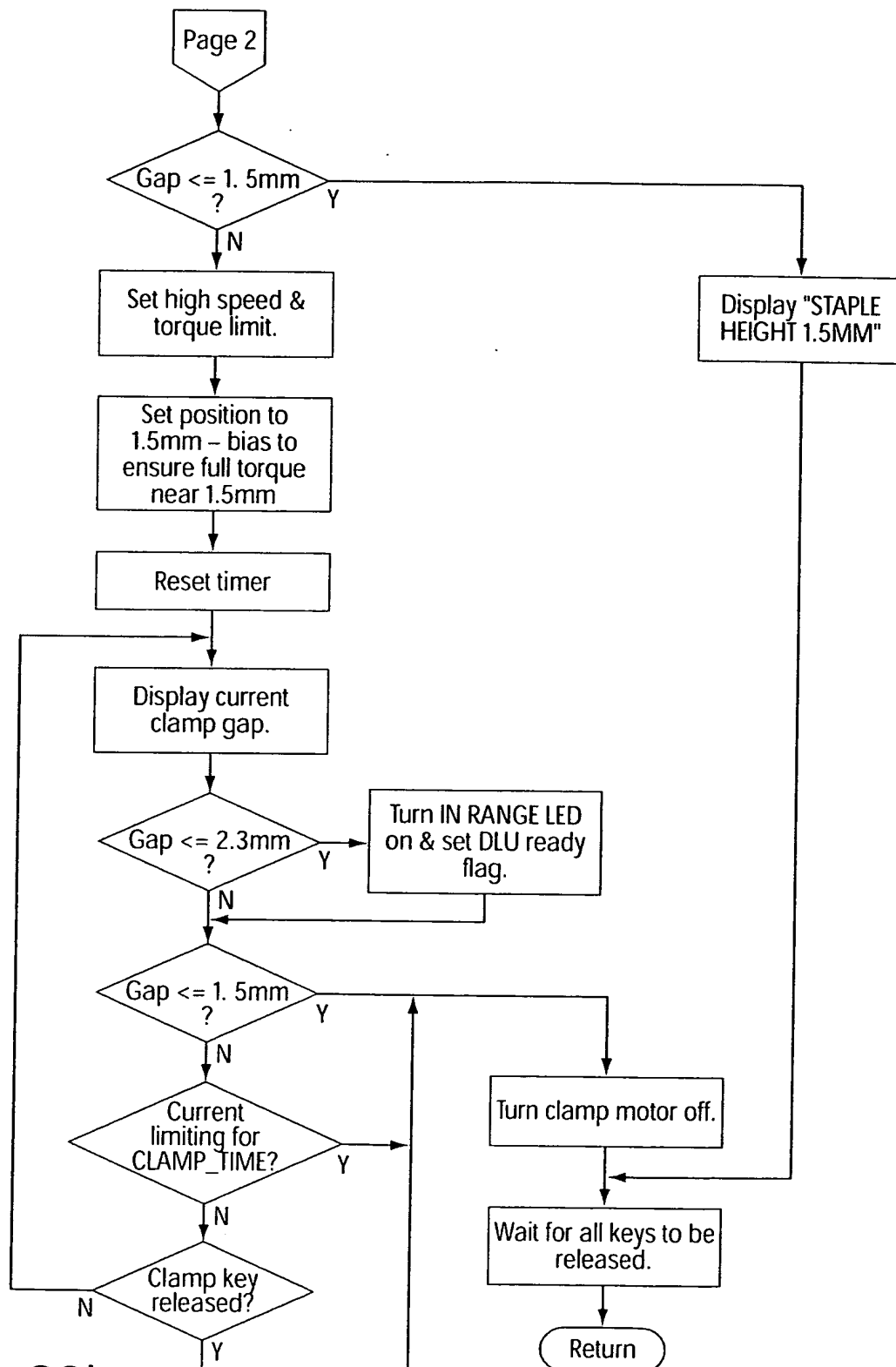
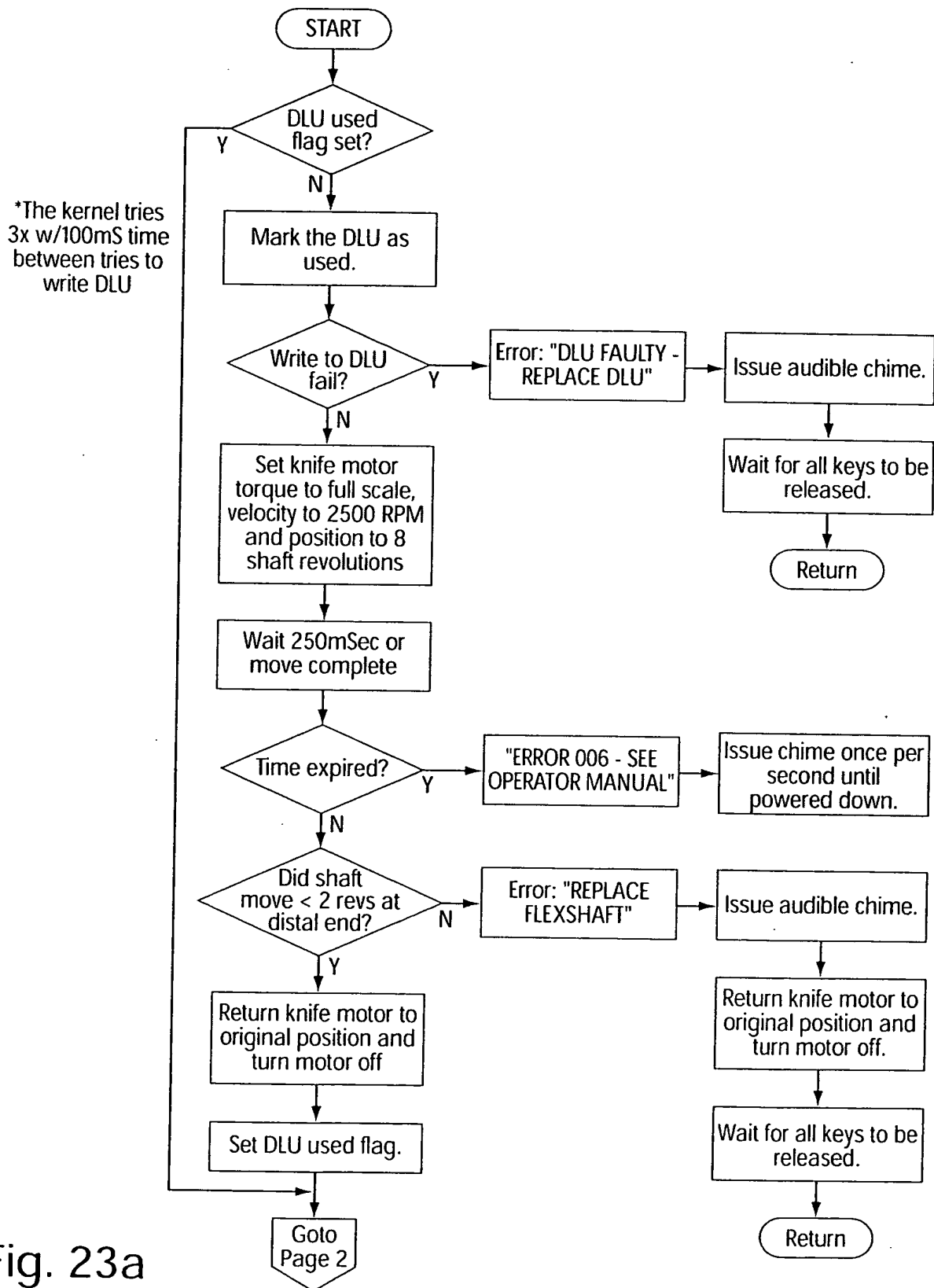


Fig. 22b



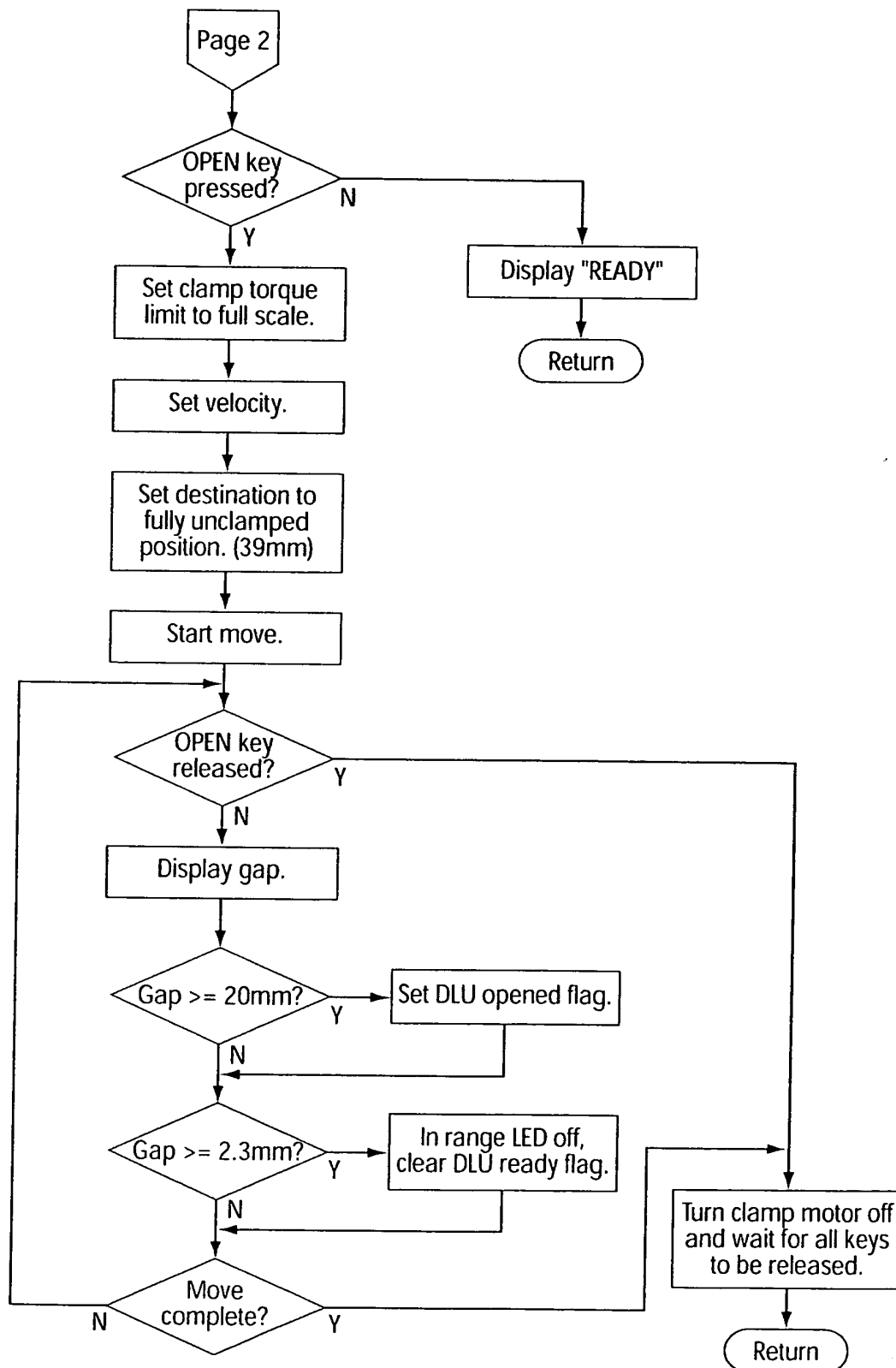


Fig. 23b